

Compal Confidential

ZAMB0/ZAMC0 M/B Schematics Document

AMD Kaveri(FP3) + Bolton(M3)

AMD TOPAZ S3

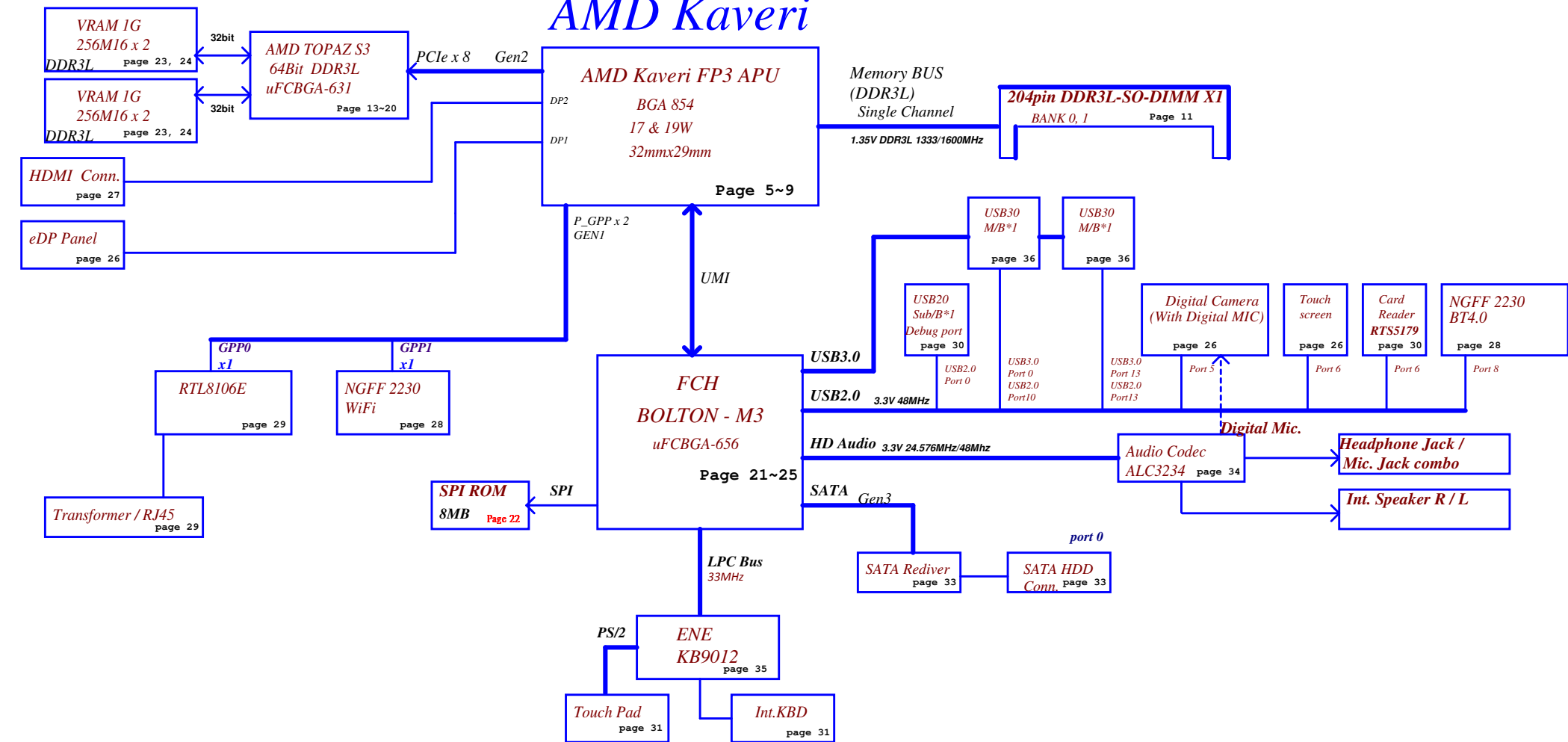
2014-2-24

REV : 0.2

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Model Name : ZAMB0/ZAMC0

AMD Kaveri



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RTC CKT.
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Power On/Off CKT.
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Fan Control
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DC/DC Interface CKT.
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Power Circuit
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Sub board

LID SW - Power/B
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D/B
-USB20 x1
-Card Reader
SD/MMC 2 IN 1
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Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+VDDCI	0.95-1.0V switched power rail	PX5	OFF	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+VGA_PCIE	0.95V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail for APU	ON	OFF	OFF	OFF
+1.35V	1.35V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+3VGS	3.3V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	PX5	OFF	OFF	OFF
+1.8VS	1.8V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3VALW	3.3V power rail for FCH	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN_NGFF	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Fintek thermal sensor	1001 101X b	9AH
Charger IC	0001 001X b	09H	SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
MINI CARD					

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64

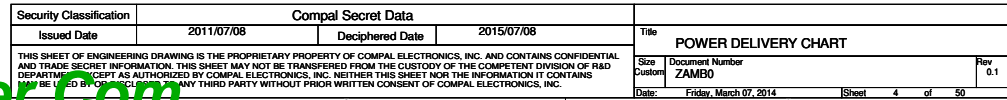
BOARD ID Table

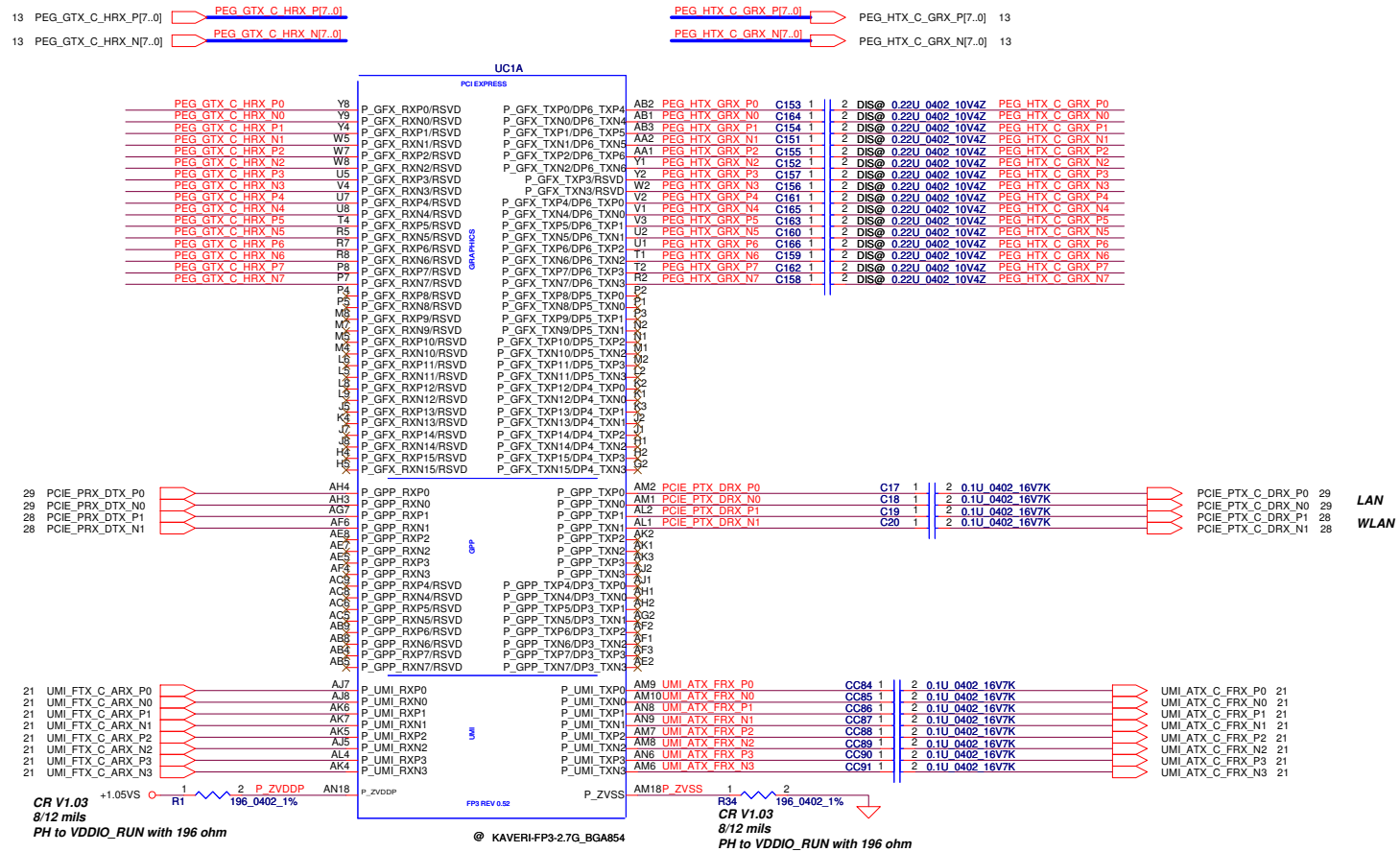
Board ID	UMA	DIS (Topaz)
0	SSI	
1		SSI
2	PT	
3		PT
4	ST	
5		ST
6	1.0	
7		1.0

BOM Option Table

BOM Structure	Description	UMA 43XX	OPAL 43XX	JET 43XX															
9022@	Use EC 9022																		
9012@	Use EC 9012	V	V																
UMA@	Display output from APU (UMA only)	V	V																
VGA@	Use VGA (PX or DIS only)		V																
EDP@	Use eDP Panel		V																
AL@	Use Auto load EC code function																		
AC@	Support AC Function																		
NOAC@	No Support AC Function																		
		V	V																
CONN@	Connector (Control by ME)	V	V																
HDT@	Debug Connector																		
EMC@	EMC Component																		
XEMC@	Reservec for EMC																		
X76@	VRAM ID Table (Load By X76J)																		
128@	VRAM x 8pcs																		
OPAL@	ATI OPAL VGA CONTROLLER																		
JET@	ATI JET VGA CONTROLLER																		
BL@	ATI JET VGA CONTROLLER																		
@	Unpop																		
TS@	Touch Screen																		
NEMI@	Unpop EMI																		
NESD@	Unpop ESD																		
AOAC@	AOAC Function																		
NAOAC@	Non AOAC Function																		

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A8-7100 AM7100ECH44JA 1.8G BGA 854P APU A10-7300 AM7300ECH44JA 2G BGA 854P APU FX-7500 FM7500ECH44JA 2.1G BGA 854P APU

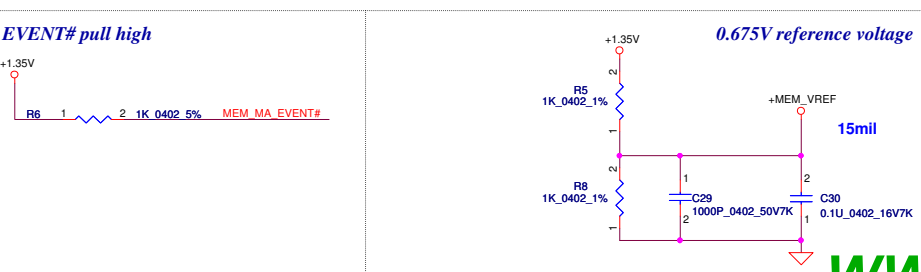
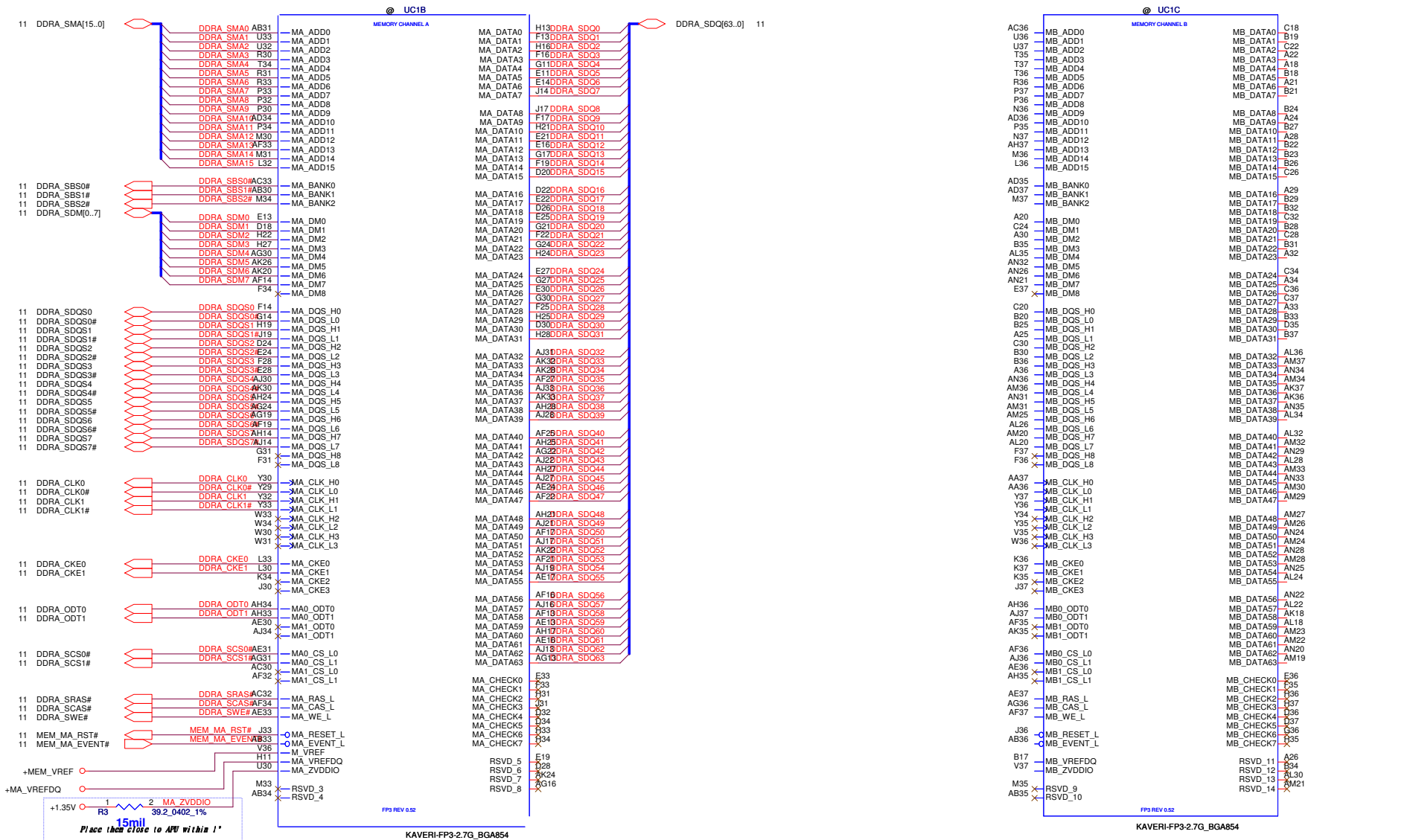
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SA00007S30L

SA00007TT0L

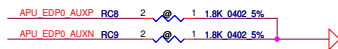
AMD, FX-7500, KAVERI, PR	SA00007TT0L	S IC FX-7500 FM7500ECH44JA 2.1G BGA 854P APU
AMD,A10-7300, KAVERI, PR	SA00007S30L	S IC A10-7300 AM7300ECH44JA 2G BGA 854P APU
AMD A8-7100, KAVERI, PR	SA00007S20L	S IC A8-7100 AM7100ECH44JA 1.8G BGA 854P APU

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If not used, pins are left unconnected (DG ref.)

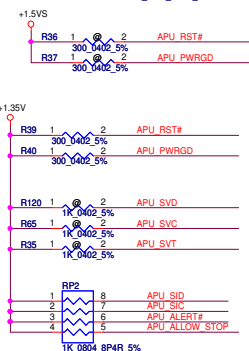
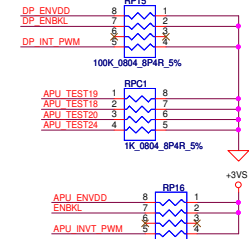
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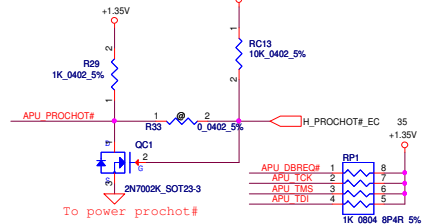
Place near APU

Place near APU

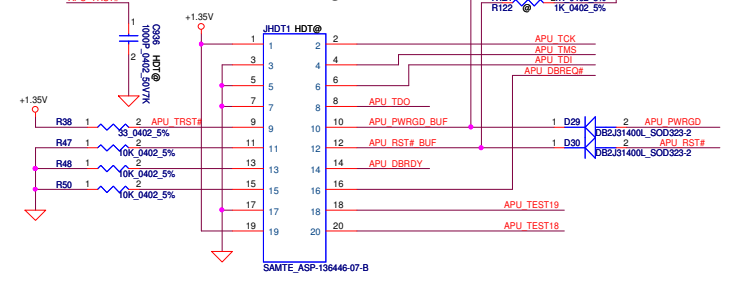
To eDP Conn



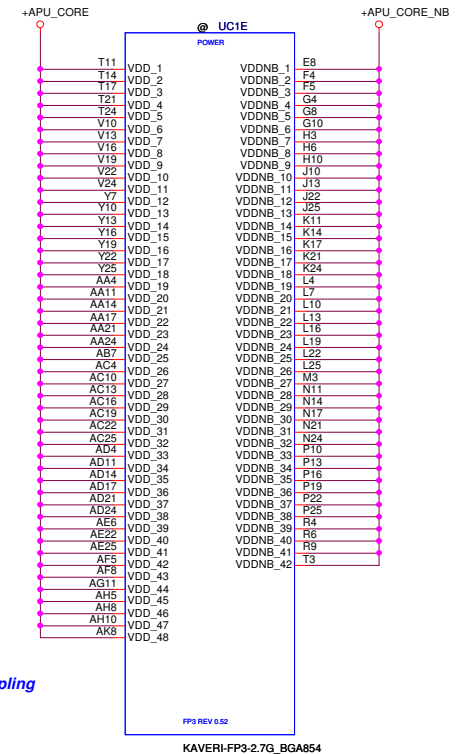
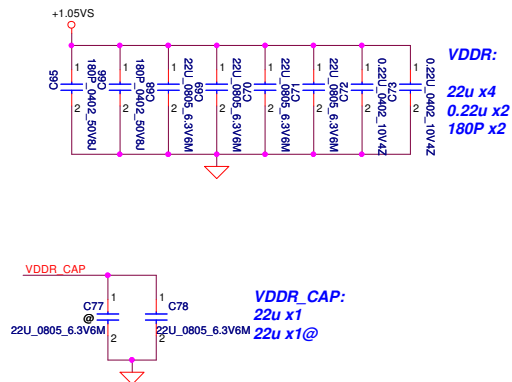
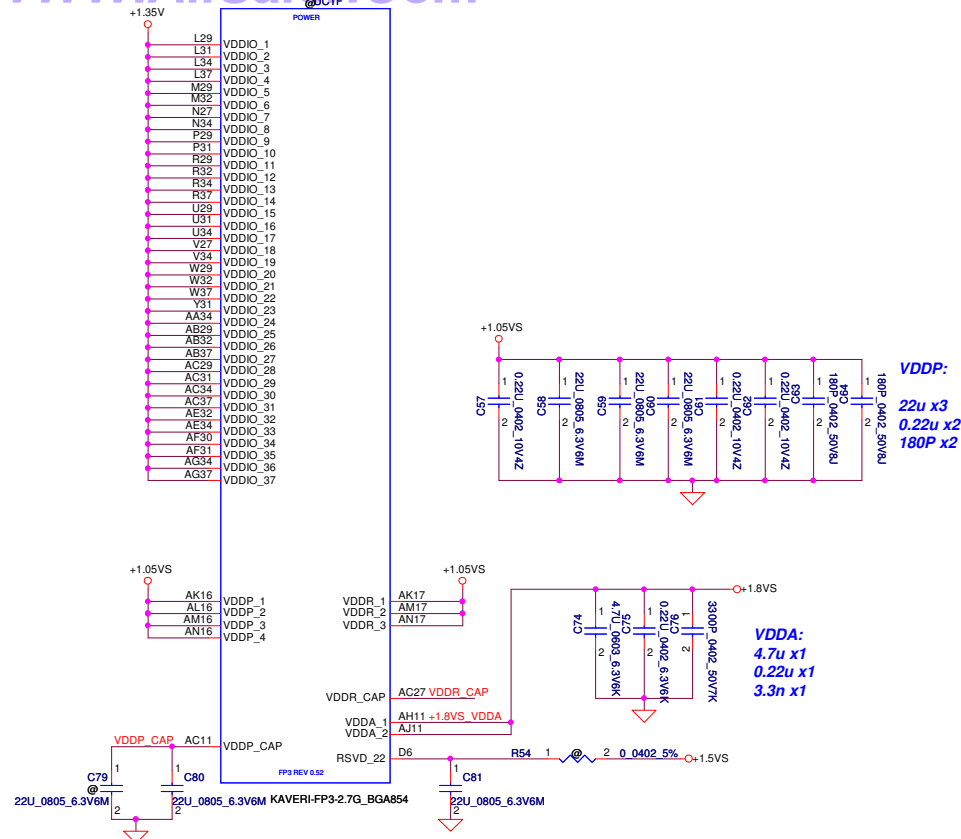
Asserted as an input to force the processor into the HTC-active state



HDT+ Debug conn



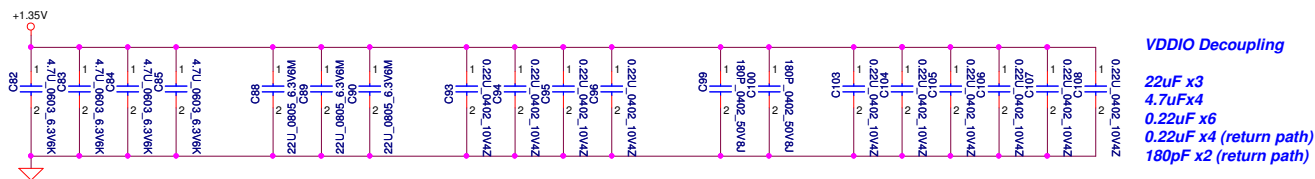
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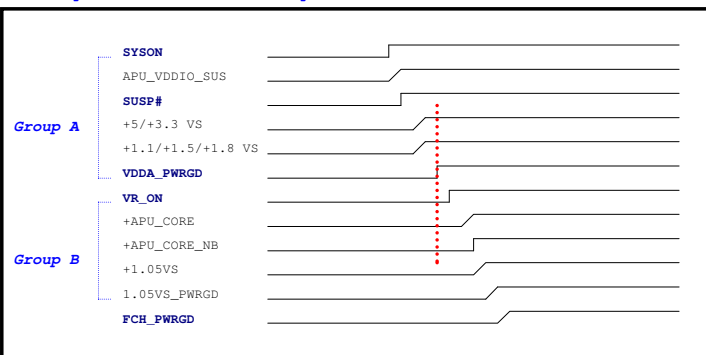
Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.35V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A

+APU_CORE_NB
Decoupling
Power Side
22uF x10 @ x2
0.22uF x3
180pF x4

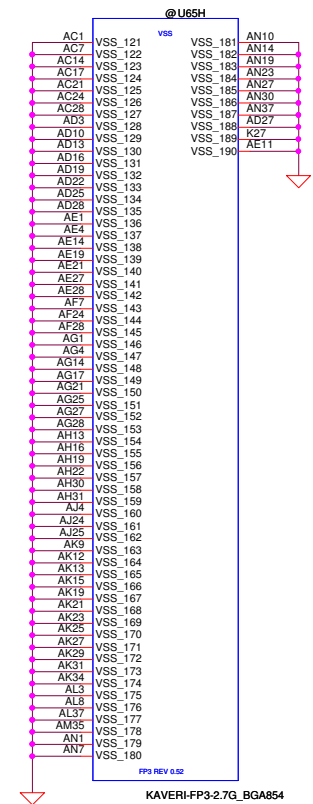
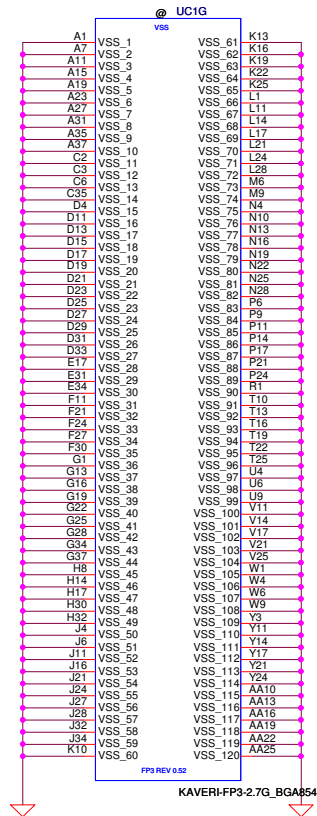
Check list CH47
+APU_CORE Decoupling
Power Side
22uF x11 @ x2
0.22uF x2
0.01uF x3
180pF x3



APU sequence : GROUP A need ramp before GROUP B

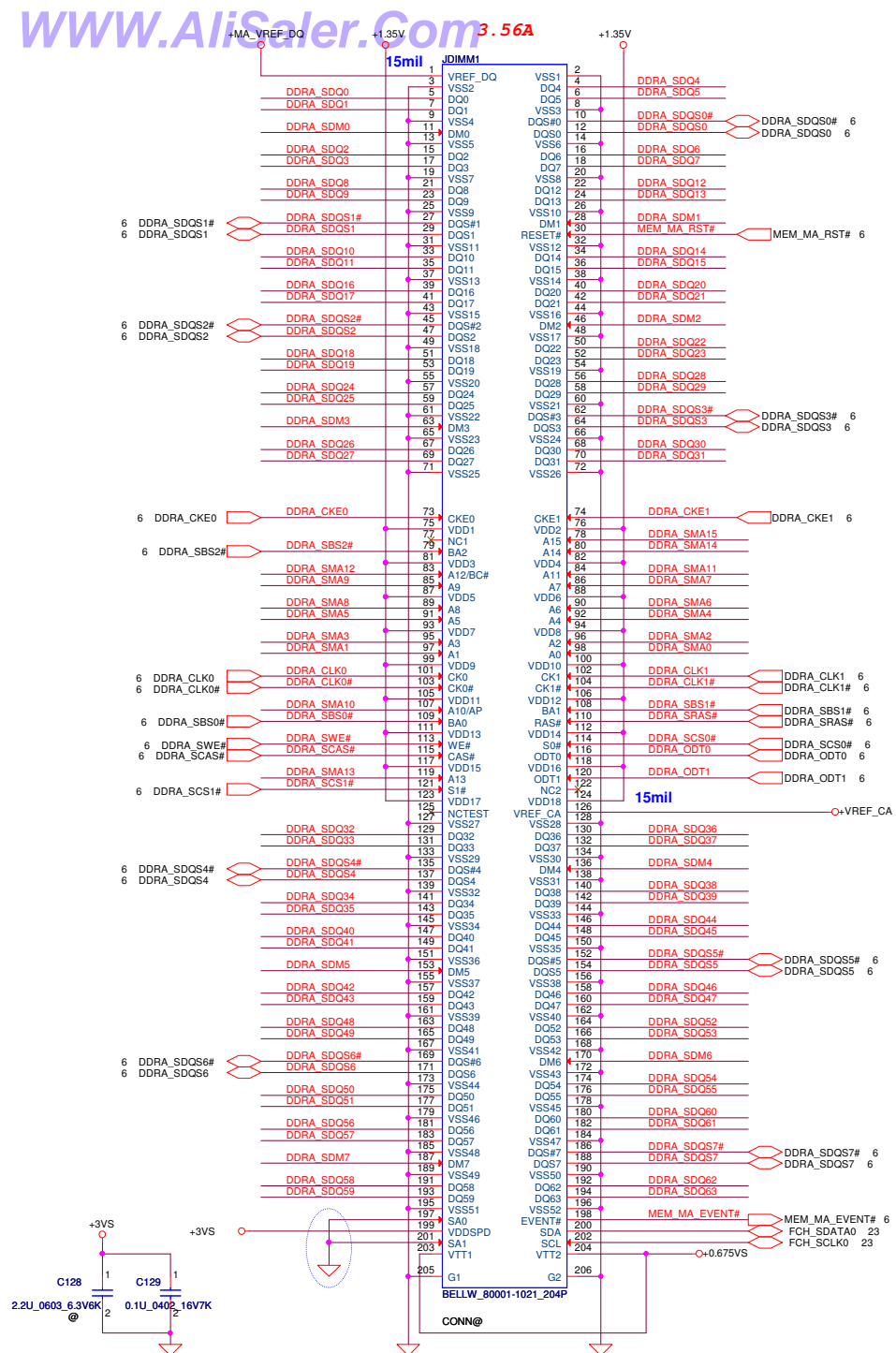


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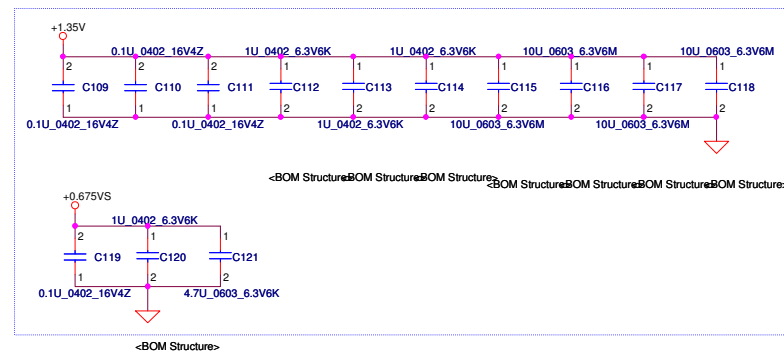
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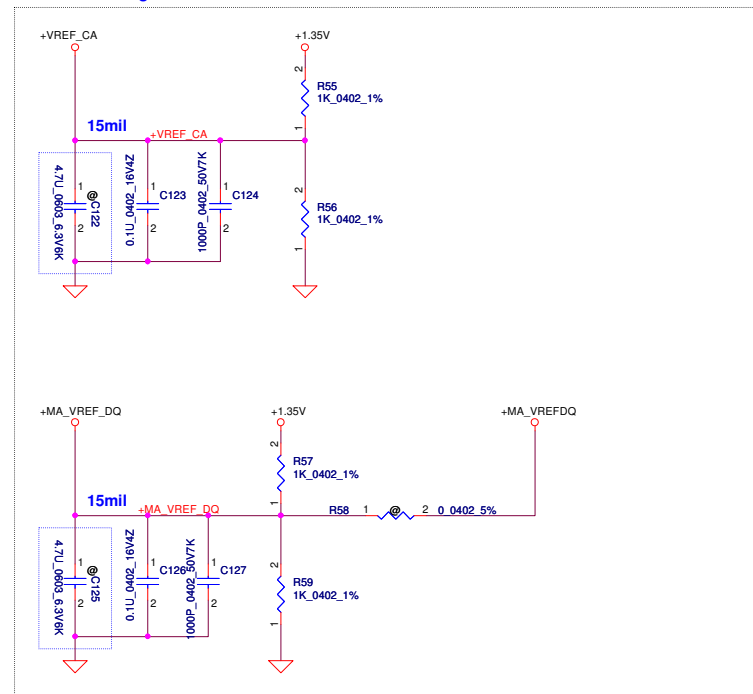
DIMM_A STD H:4mm
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Place near DIMM1



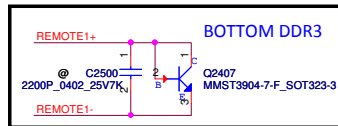
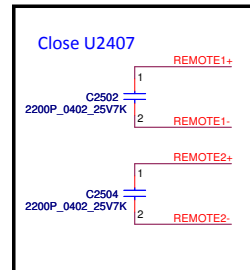
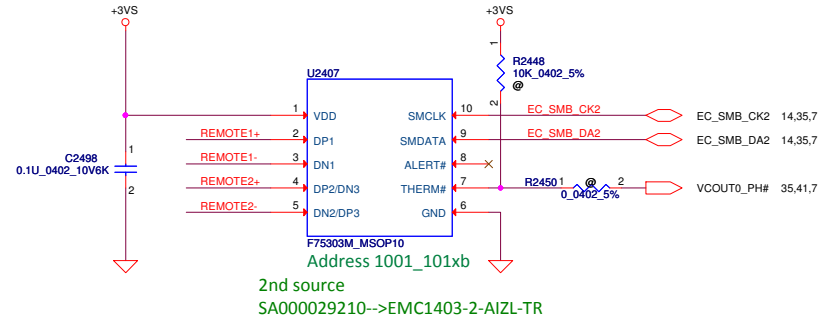
Follow CRB design



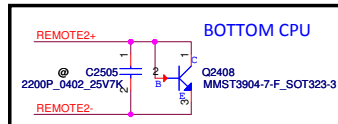
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Fintek thermal sensor placed near by DDR3

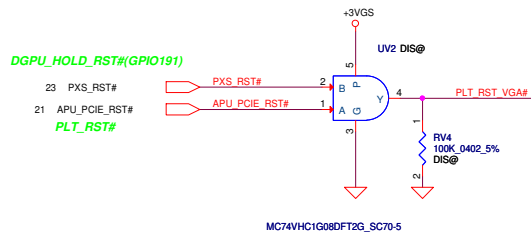
SA000046C00(S IC EMC1403-2-AIZL-TR MSOP 10P SENSOR)



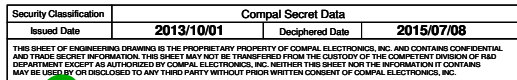
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"









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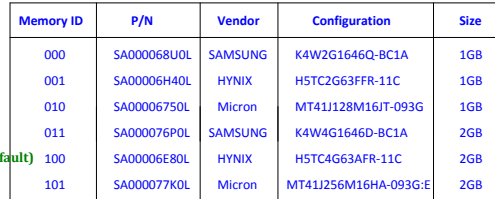


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Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

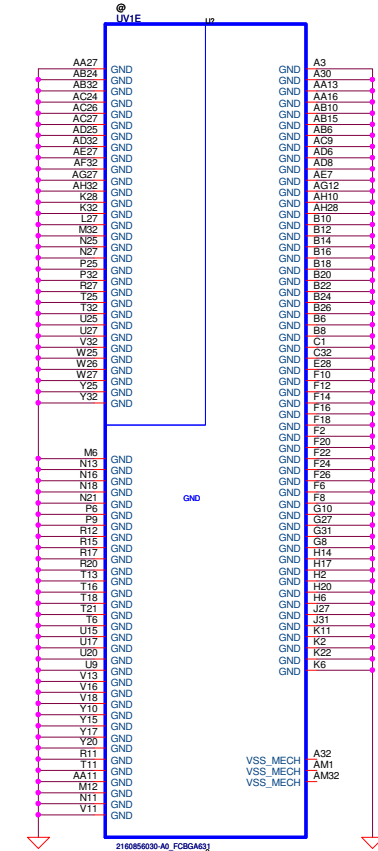
0402_1% AZ0	RV15 2G_5@  6.98K_0402_1% SD003402680	RV16 2G_5@  4.99K_0402_1% SD034499180
0402_5%	RV15 2G_1@  4.53K_0402_1% SD034453180	RV16 2G_1@  4.99K_0402_1% SD034499180
0402_5%	RV15 2G_M@  3.24K_0402_1% SD034324180	RV16 2G_M@  5.62K_0402_1% SD034562180



SS1 (default)

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U0L	SAMSUNG	K4W2G1646Q-BC1A	1GB
001	SA00006H40L	HYNIX	H5TC2G63FFR-11C	1GB
010	SA00006750L	Micron	MT41J128M16JT-093G	1GB
011	SA000076P0L	SAMSUNG	K4W4G1646D-BC1A	2GB
100	SA00006680L	HYNIX	H5TC4G63AFR-11C	2GB
101	SA000077K0L	Micron	MT41J256M16HA-093G:E	2GB

JP9 DEFAULT SHORT



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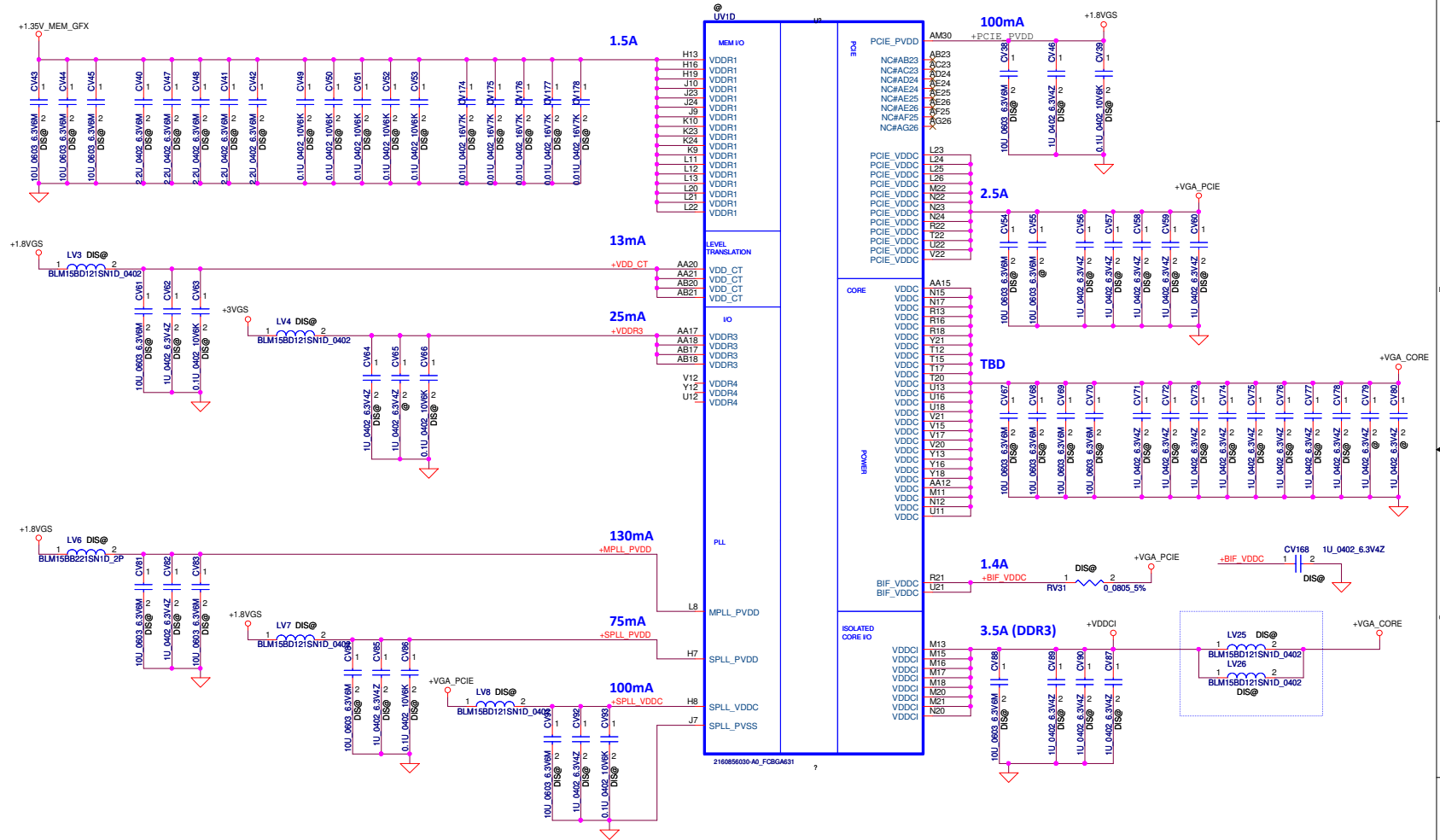
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+VGA_PCIE	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	1
SPLL_VDDC	100mA	1	1

+1.35V_MEM GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 1.5A	3	5	5	5

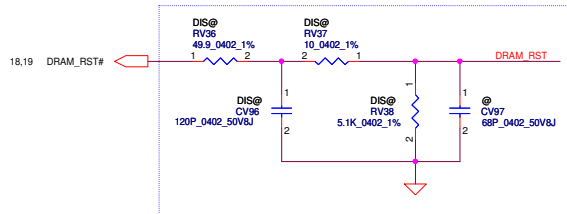
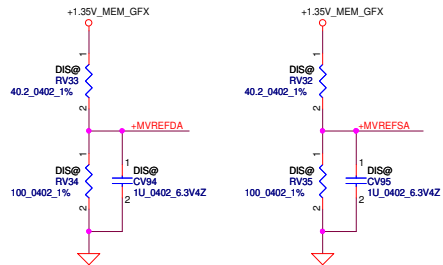
+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4 (300mA)	0	0	0
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1

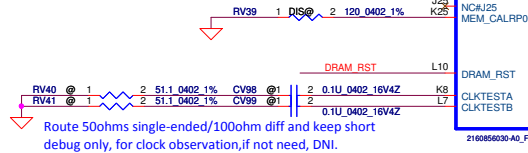


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				Document Number	ZAMBO
				Date	Friday, March 07, 2014
				Sheet	16 of 50

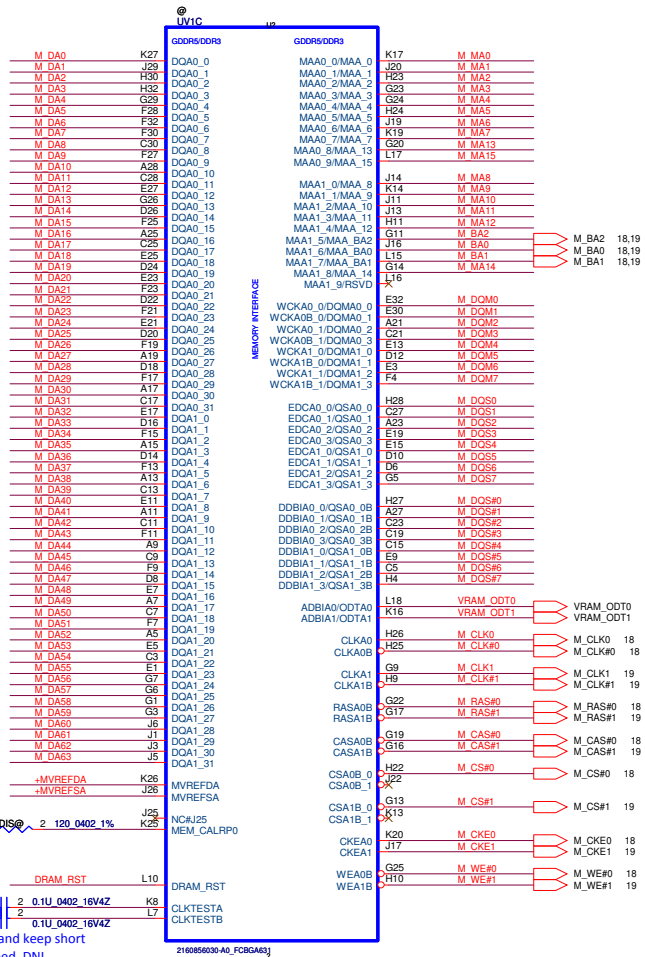
18,19 M_DA[63..0] M_DA[63..0]
 18,19 M_MA[15..0] M_MA[15..0]
 18,19 M_DM[7..0] M_DM[7..0]
 18,19 M_DS[7..0] M_DS[7..0]
 18,19 M_DGS[7..0] M_DGS[7..0]



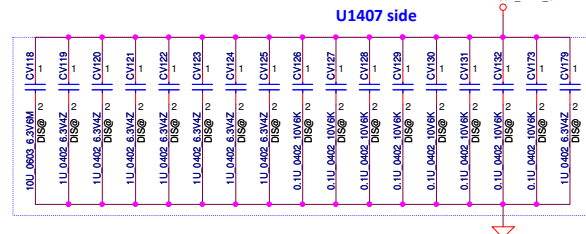
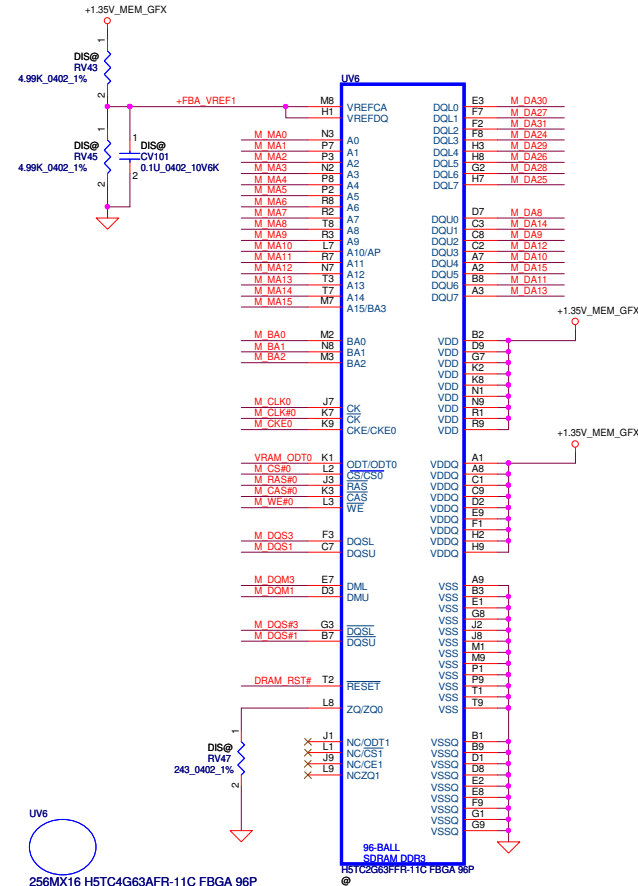
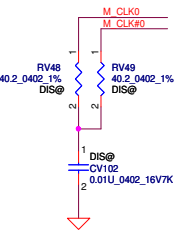
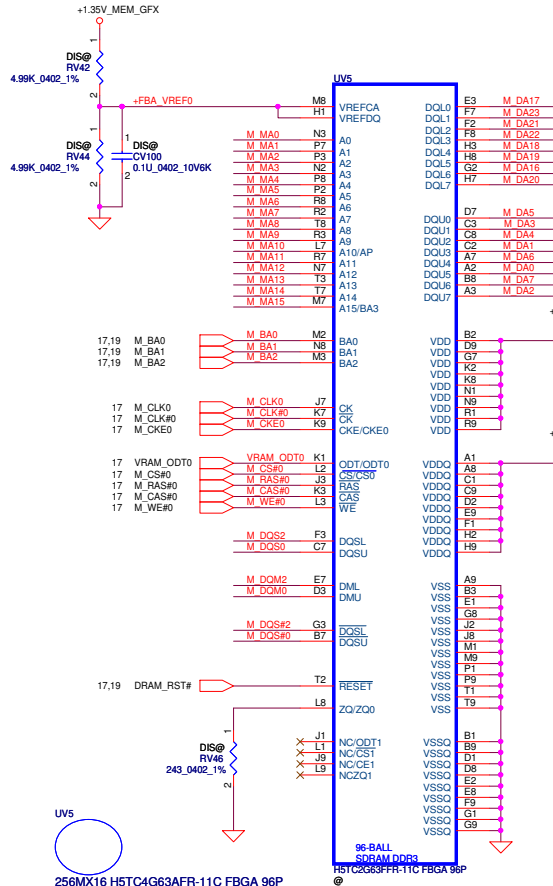
Place close to GPU (within 25mm)
 and place component close to each other



Route 50ohms single-ended/100ohm diff and keep short
 debug only, for clock observation, if not need, DNI.



17,19 M_DA[63..0] M_DA[63..0]
 17,19 M_MA[15..0] M_MA[15..0]
 17,19 M_DQM[7..0] M_DQM[7..0]
 17,19 M_DQS[7..0] M_DQS[7..0]
 17,19 M_DQS#[7..0] M_DQS#[7..0]



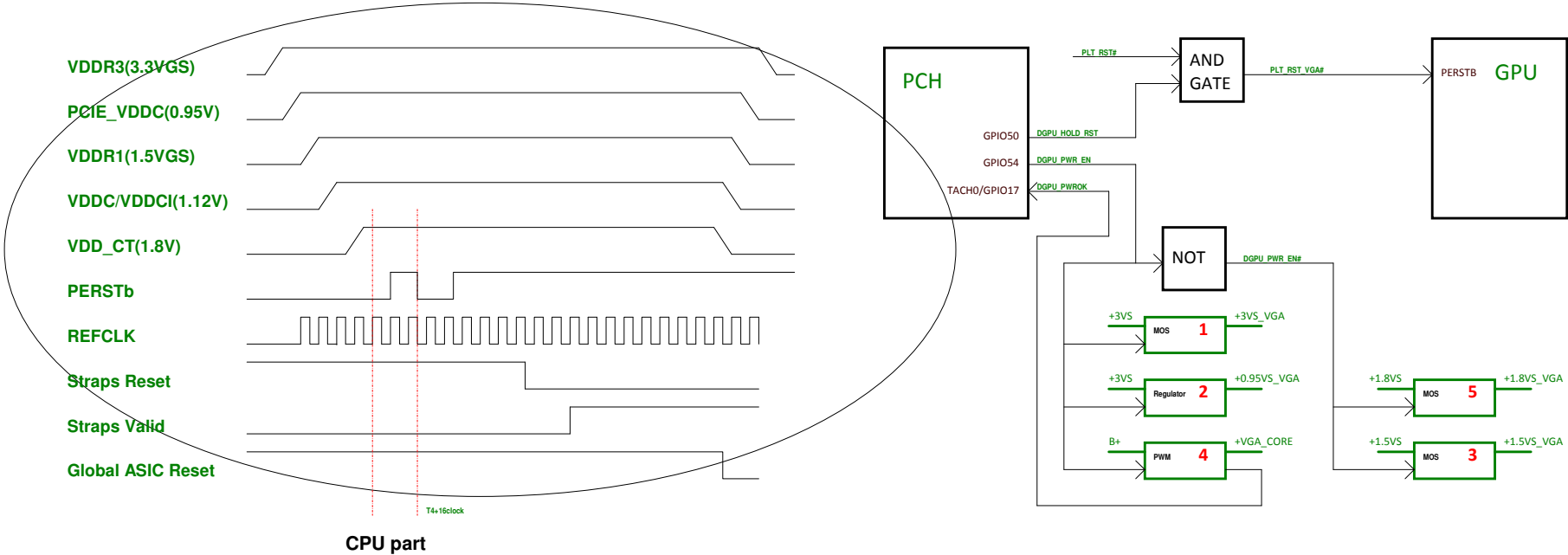
<ul style="list-style-type: none"> X7655131104, ALT. GROUP PARTS VRAM 2G HYNIX ZAVC0, A.2 (Design) SA00006E80L, S IC D3 256MX16 H5TC4G63AFR-11C FBGA 96P, A.1 (Design) SD034453180, S RES 1/16W 4.53K +-1% 0402, A.1 (Design) SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)
<ul style="list-style-type: none"> X7655131105, ALT. GROUP PARTS VRAM 2G SAMSUNG ZAVC0, A.2 (Design) SA000076P0L, S IC D3 256MX16 K4W4G1646D-BC1A FBGA 96P, A.2 (Design) SD000002680, S RES 1/16W 6.98K +-1% 0402, A.1 (Design) SD034499180, S RES 1/16W 4.99K +-1% 0402, A.2 (Design)
<ul style="list-style-type: none"> X7655131106, ALT. GROUP PARTS VRAM 2G MICRON ZAVC0, A.2 (Design) SA000077K0L, S IC D3 256MX16 MT41J256M16HA-093G:E FBGA, A.4 (Design) SD034324180, S RES 1/16W 3.24K +-1% 0402, A.1 (Design) SD034562180, S RES 1/16W 5.62K +-1% 0402, A.1 (Design)

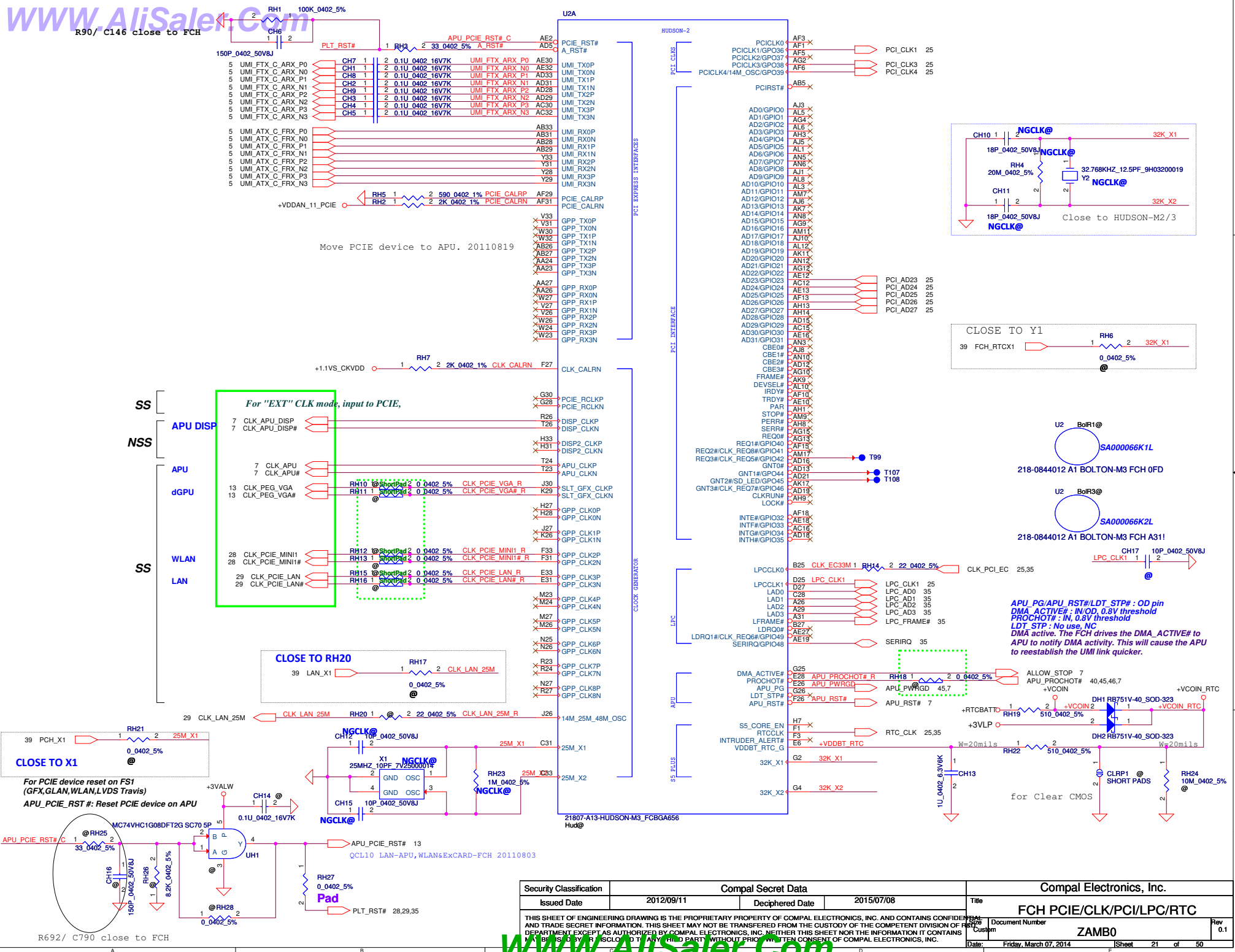
Security Classification	Compal Secret Data		Title	
Issued Date	2013/10/01	Deciphered Date	2015/07/08	TOPAZ VRAM A Lower
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Date	Friday, March 07, 2014	Sheet	18	of 50

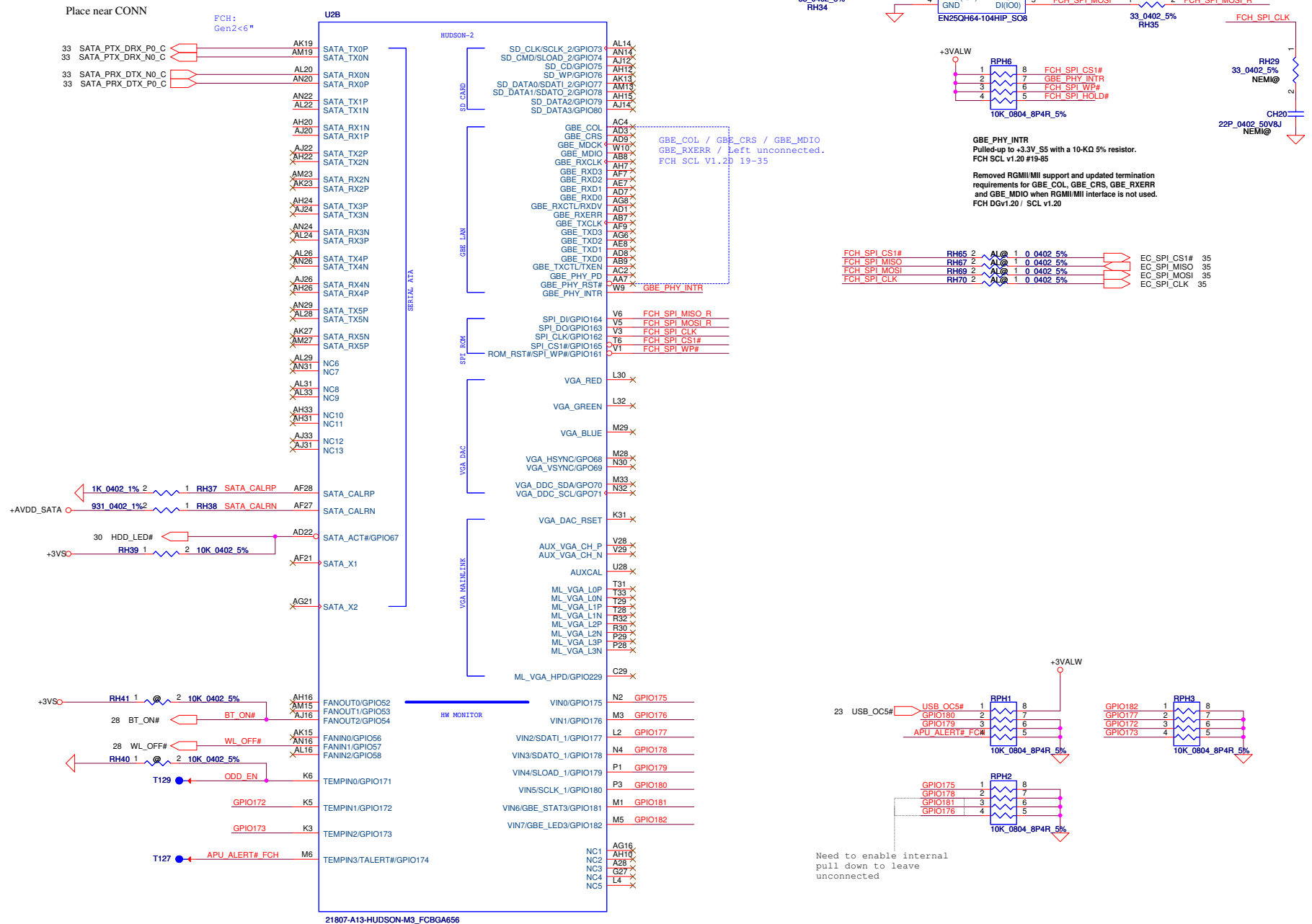
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Issued Date	2013/10/01	Deciphered Date	2015/07/08	Title	TOPAZ VRAM A Upper
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				Custom	0.1
				ZAMBO	
Date:	Friday, March 07, 2014	Sheet	19	of	50

Power-Up/Down Sequence

- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- 2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- 3. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- 4. For power down, reversing the ramp-up sequence is recommended.

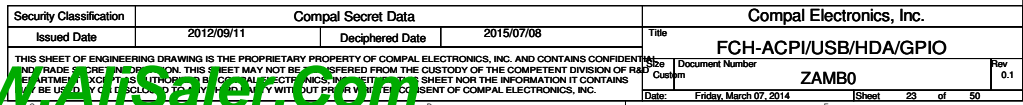


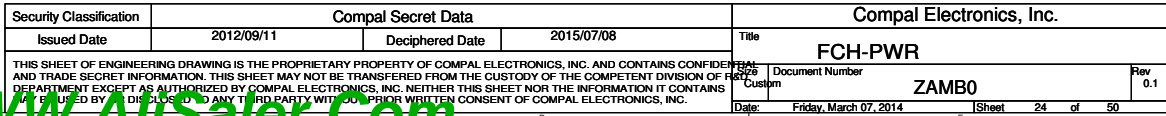




Hud@

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Date: Friday, March 07, 2014				Sheet	22 of 50





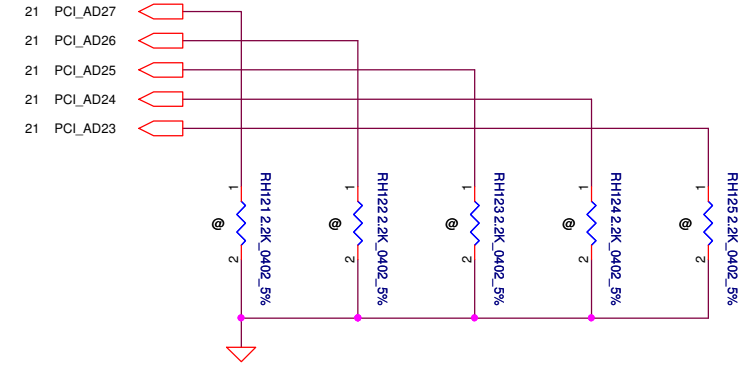
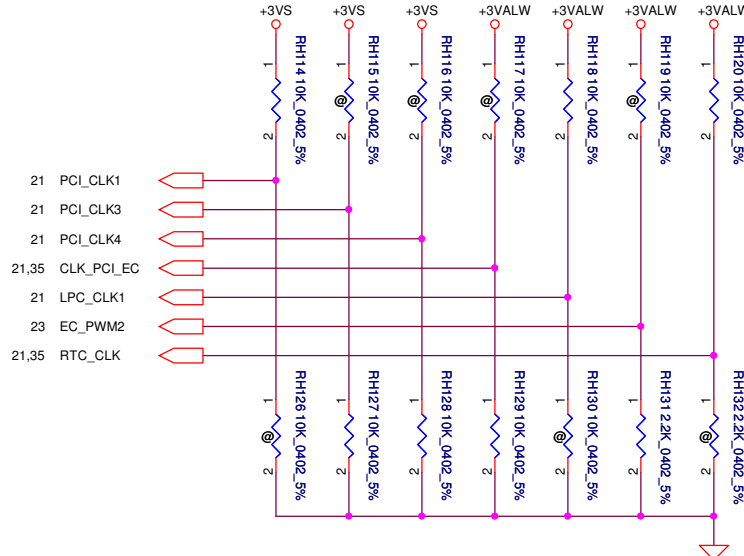
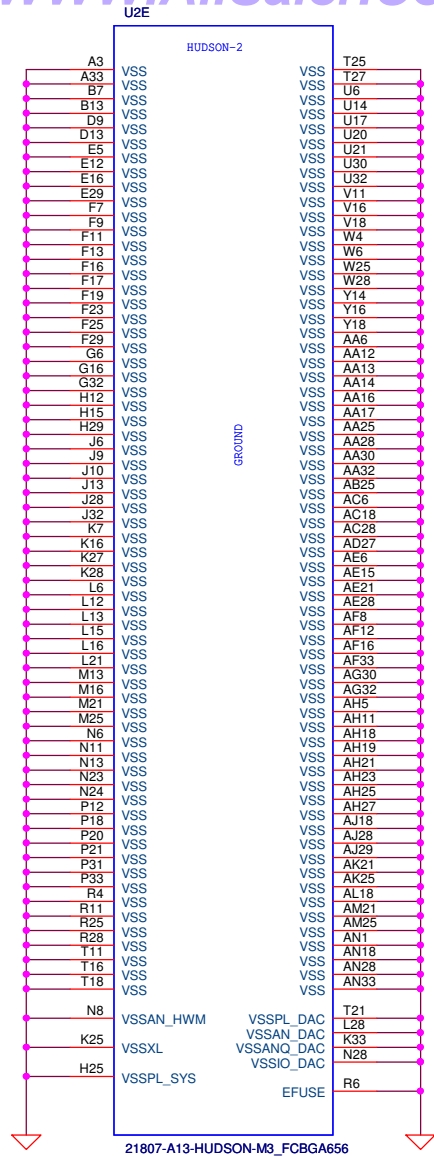
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

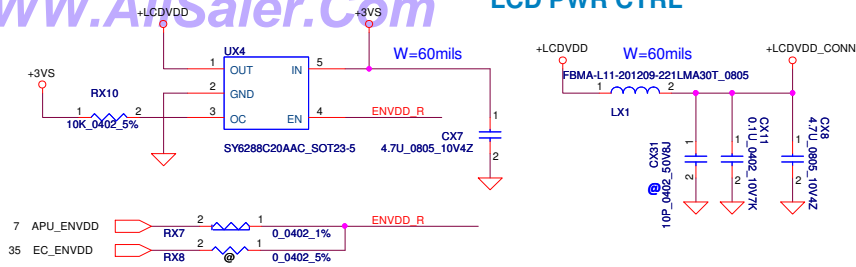
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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				Date:	Friday, March 07, 2014	Sheet 25 of 50

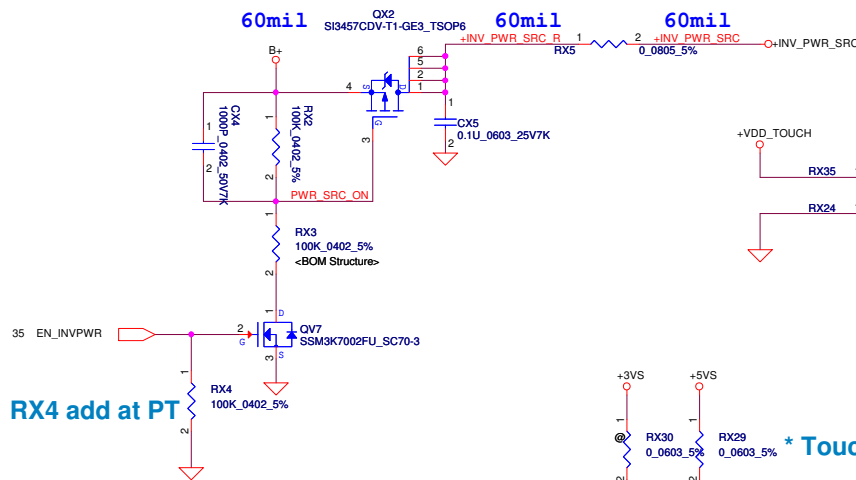
LCD PWR CTRL



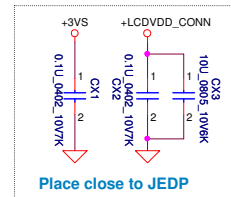
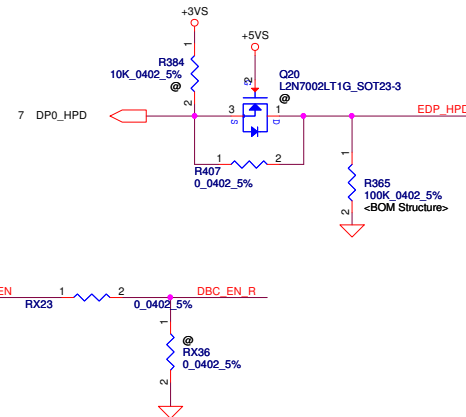
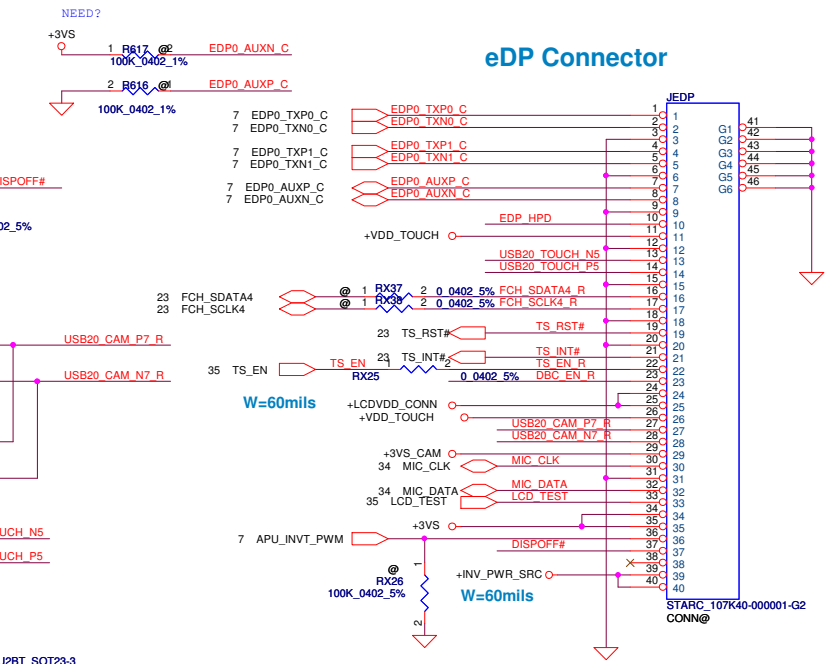
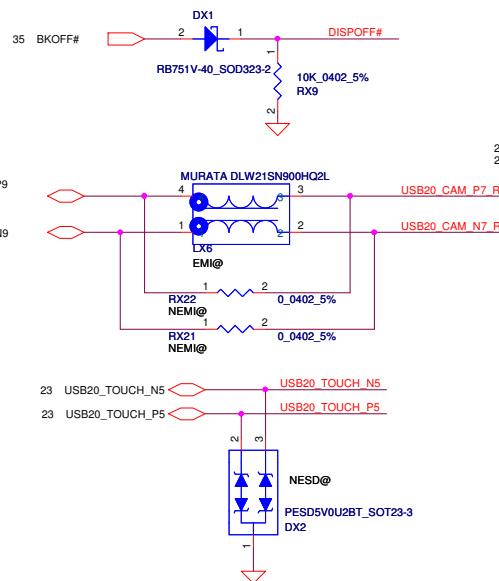
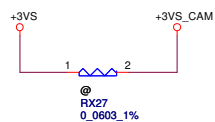
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

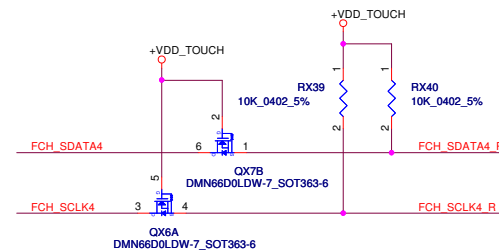
LCD backlight PWR CTRL



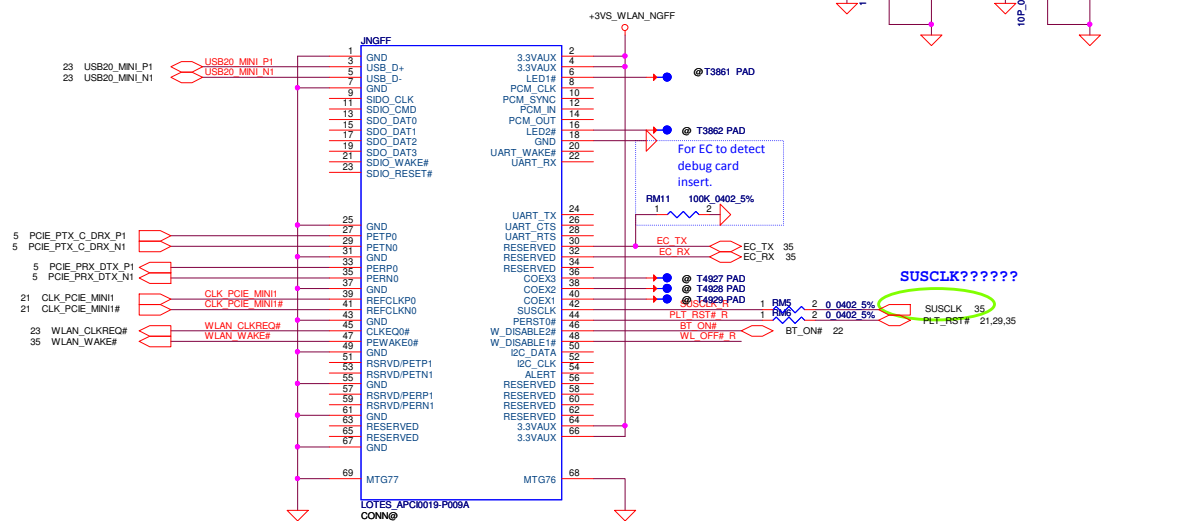
Webcam PWR CTRL



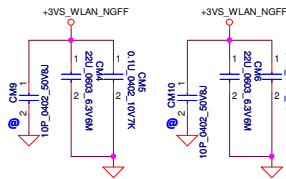
Place close to JEDP



NGFF WL Con (E Key)

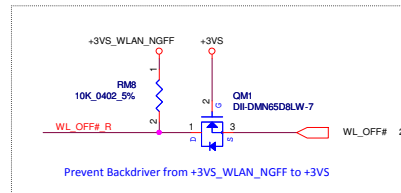
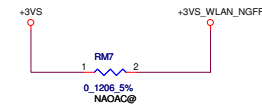


closed to pin 2, 4

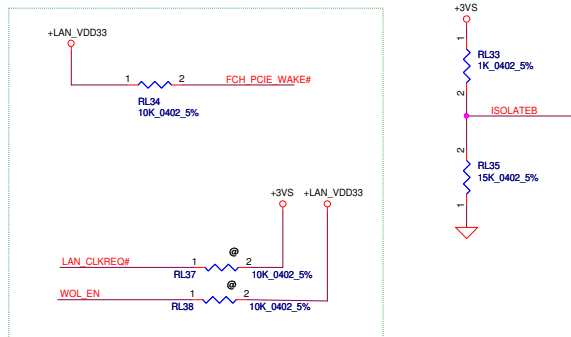
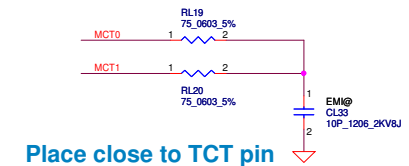
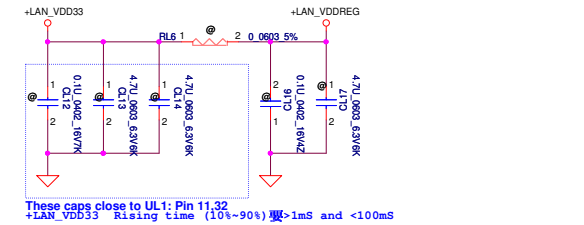


closed to pin 64, 66

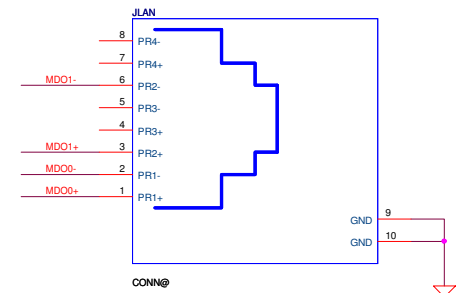
+3VALW TO +3VS_WLAN_NGFF



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				Date	Friday, March 07, 2014
				Sheet	28 of 50

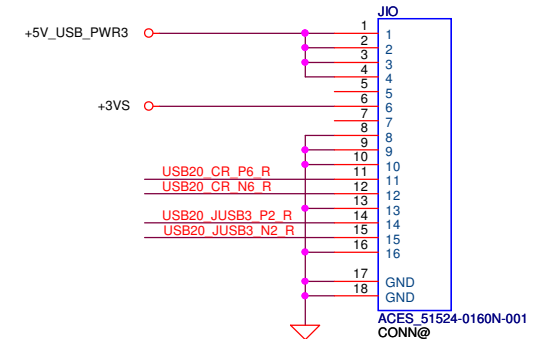
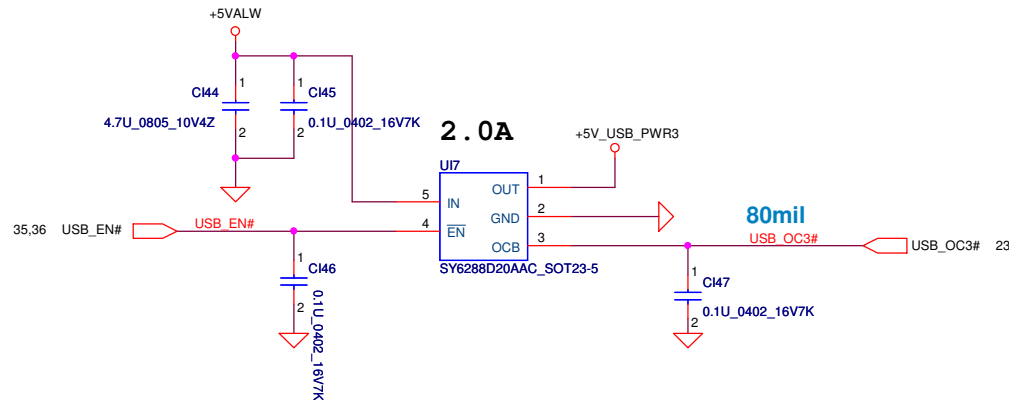


XTAL

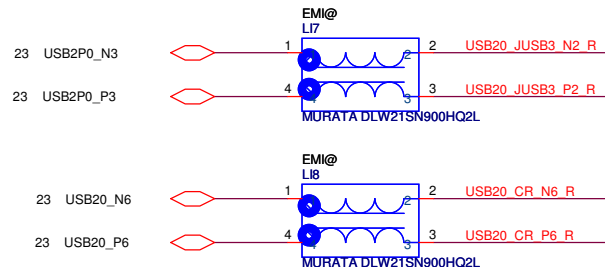


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IO to MB CONN Substitute:SP01001FS00

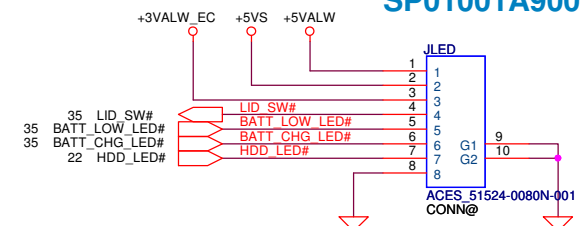


USB Conn DEBUG Port



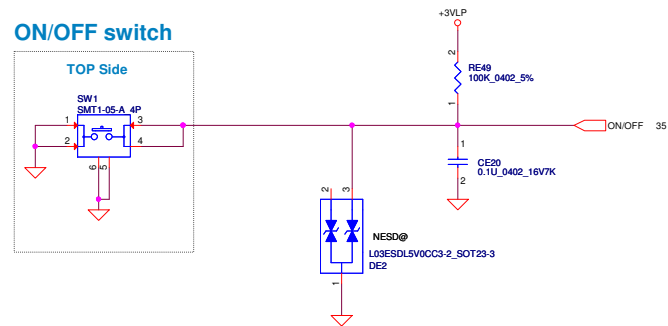
Card Reader

LED/B TO M/B SP01001A900



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				Document Number	0.1
				Date:	Friday, March 07, 2014
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Power ON Circuit

[illegible]

The diagram illustrates the internal wiring of the ACES 51524-0080N-001 connector. It shows a 23-pin connector on the left and a 10-pin connector on the right. The internal components include resistors (RES336, RES337, RES29, RES28), capacitors (C1, C2), and a JTP component. The wiring is color-coded: red for power (+3V_{TOUCH}), blue for data (FCH_SDATA1_TP, FCH_SCLK1_TP), green for control (TP_INT#, TP_WAKE, TP_DATA, TP_CLK), and yellow for ground. The diagram also shows the connection to a CE58 1U_0402_6.3V8K capacitor and a ground connection.

Key components and connections shown in the diagram:

- Power Supply:** +3V_{TOUCH} connected to pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Data Lines:** FCH_SDATA1_TP (pin 23) and FCH_SCLK1_TP (pin 23) connected to pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Control Lines:** TP_INT# (pin 23), TP_WAKE (pin 35), TP_DATA (pin 35), and TP_CLK (pin 35) connected to pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Resistors:** RES336 (10K_0402_5%), RES337 (10K_0402_5%), RES29 (100K_0402_5%), and RES28 (100K_0402_5%) are connected between pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Capacitors:** C1 (100K_0402_5%) and C2 (100K_0402_5%) are connected between pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Ground:** Connected to pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Connector:** JTP (J1) with pins 1, 2, 4, 5, 6, 7, 8, 9, 10, and 11.
- Label:** ACES 51524-0080N-001

FAN Control circuit

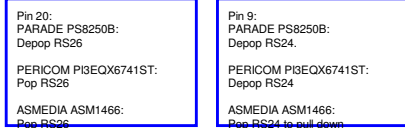
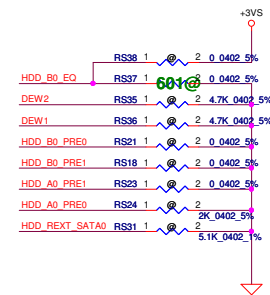
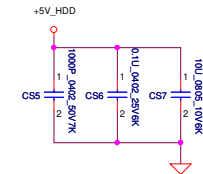
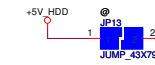
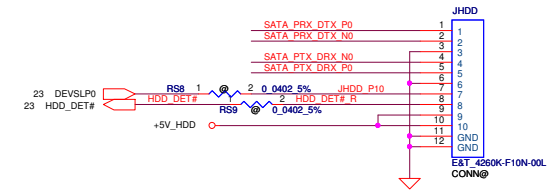
The schematic diagram illustrates a FAN Control circuit. It features two operational amplifiers: APE875M SOP 8P and ACE5 88231-03004. The APE875M is configured as a comparator, with its non-inverting input (VIN) connected to a voltage divider (2.2u 0603 6.3V6K and 100K 0402 50V7K) connected to +FAN_POWER. Its inverting input (VSET) is connected to a +5VS supply. The output (VO) of the APE875M is connected to the EN_DFAN1 pin of the ACE5 88231-03004. The ACE5 88231-03004 is configured as a relay driver, with its input (VEN) connected to a +3VS supply through a RE50 10K 0402_5% resistor. Its output (VOUT) is connected to a 40mil trace, which is then connected to the FAN_SPEED1 pin of the ACE5 88231-03004. The ACE5 88231-03004 is also connected to a +FAN_POWER supply through a 40mil trace. The circuit is powered by +FAN_POWER and +5VS supplies.

[illegible]

* Key Board Back Light

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				Custom	ZAMB0	0.1
				Date:	Friday, March 07, 2014	Sheet 32 of 50



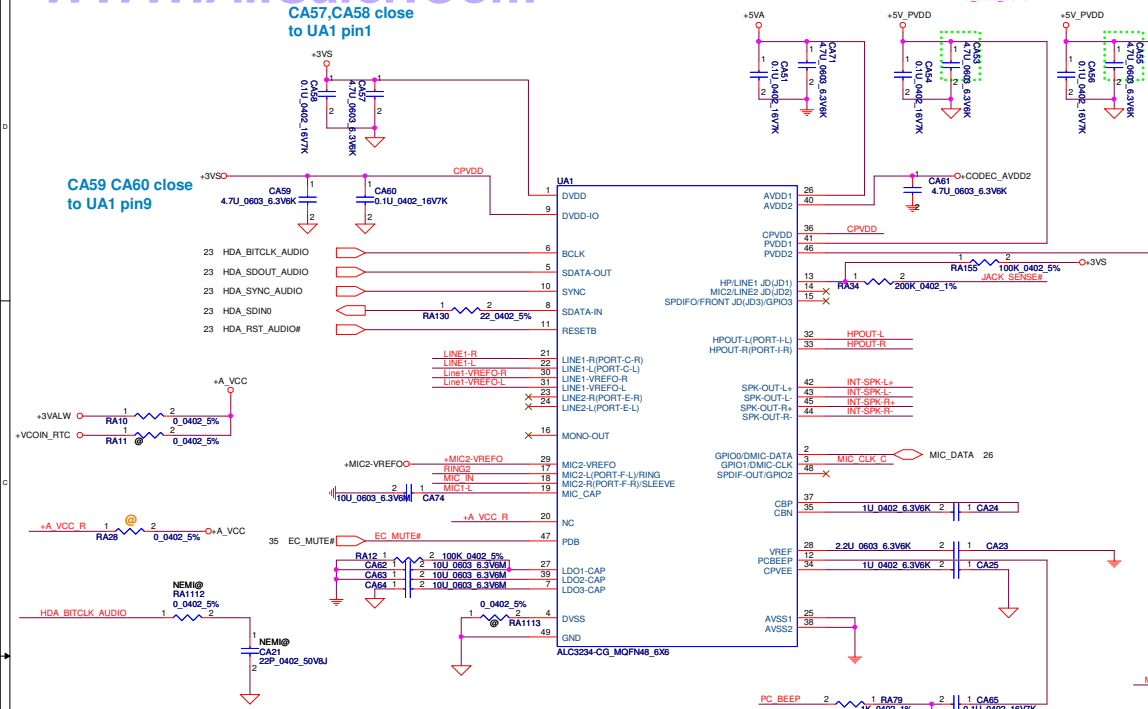
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date		2013/10/01	Deciphered Date		2015/07/08	Title
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						Document Number
ZAMBO						
Date:		Friday, March 07, 2014			Sheet 33 of 50	

CA71, CA51 place close to Pin 26

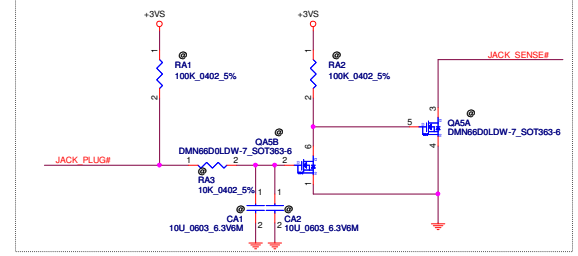
CA53, CA55 change Value from 10U_0603_6.3V6M to 4.7U_0603_6.3V6K

CA57, CA58 close to UA1 pin1

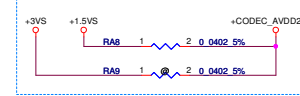
CA59 CA60 close to UA1 pin9



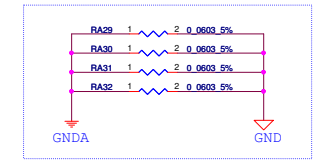
JACK_PLUG Delay circuitis



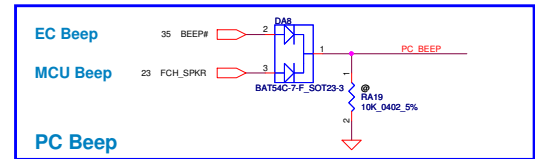
Reserve for HDA issue



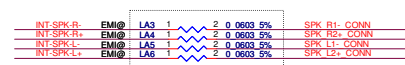
Reserve for cancel Delay circuitis



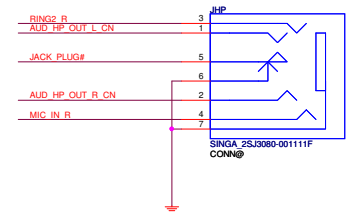
Place on the moat between GND & GNDA.



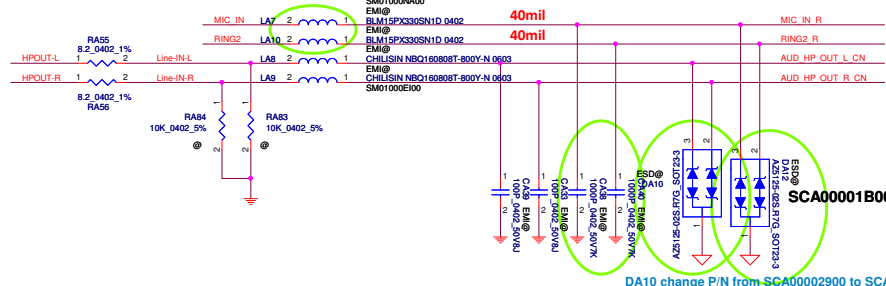
Close to UA1 Pin11,13,14,16



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

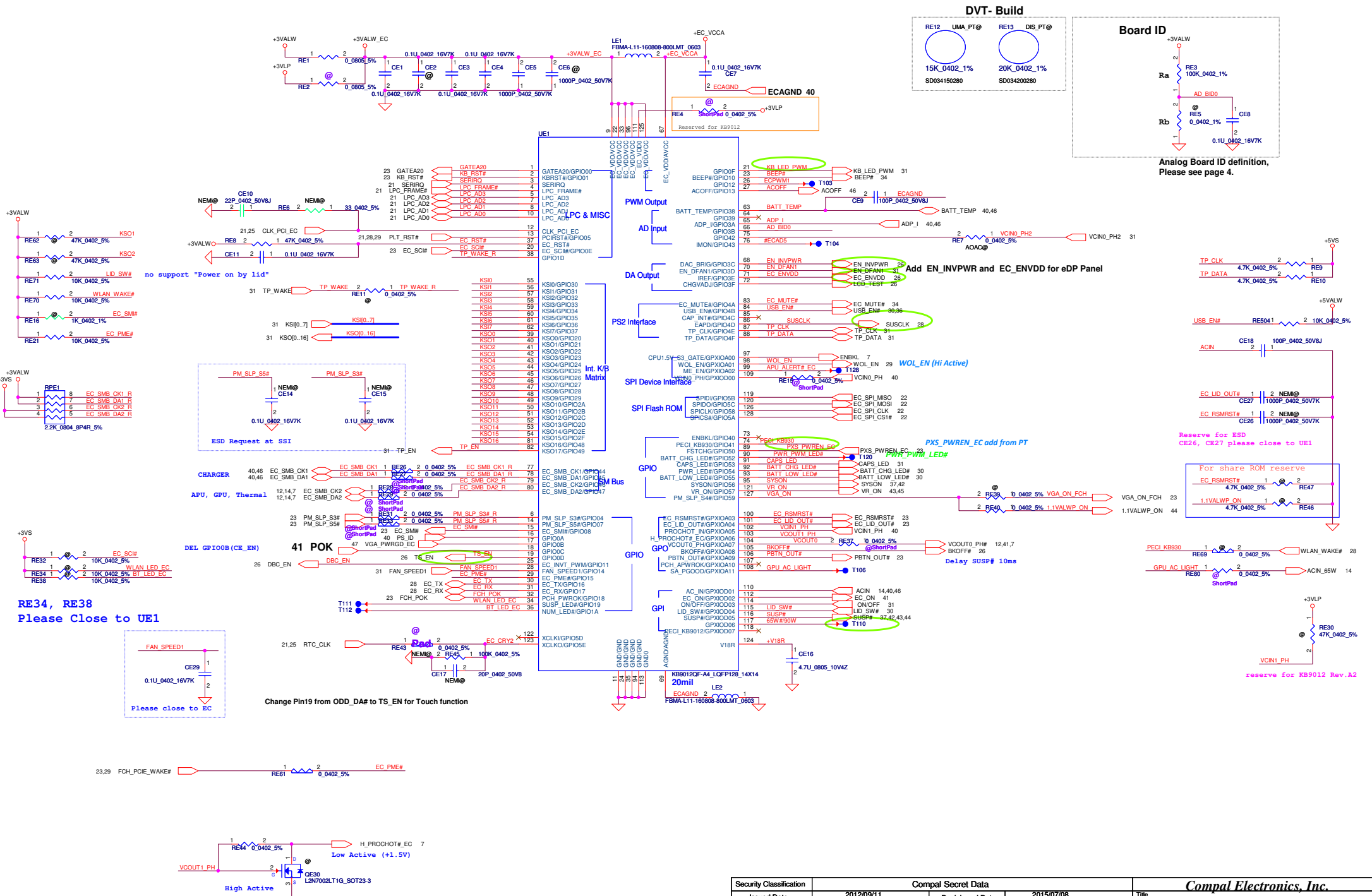


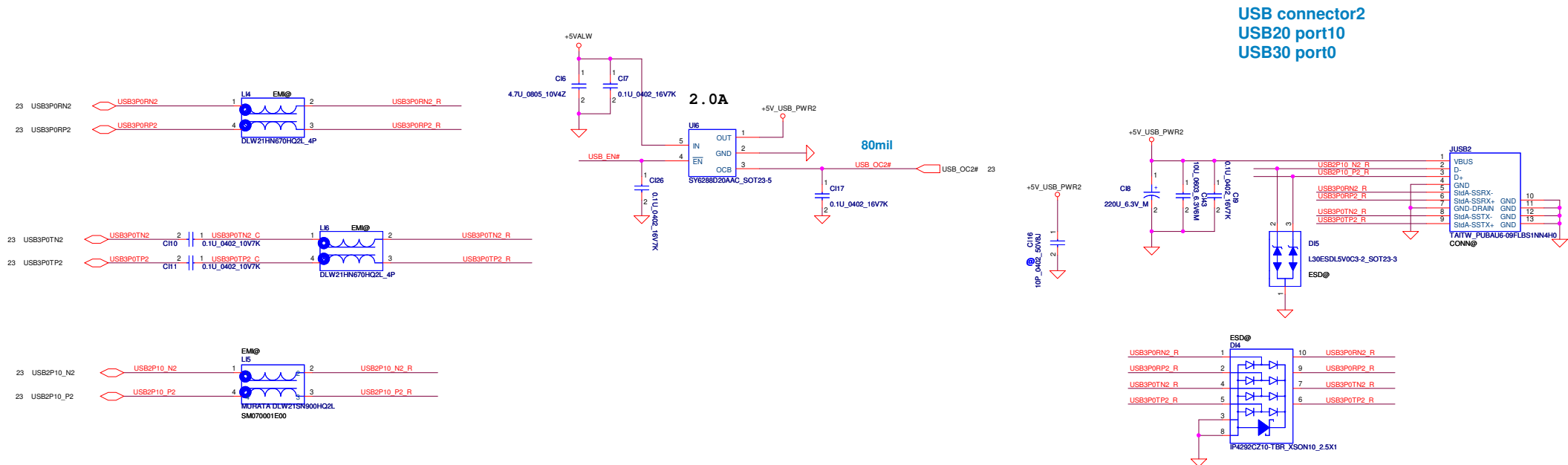
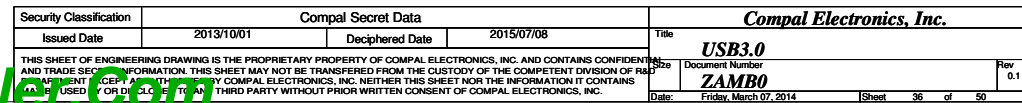
iPhone and Nokia type Combo Jack

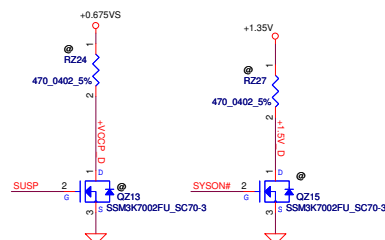
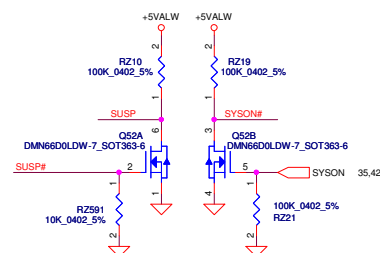
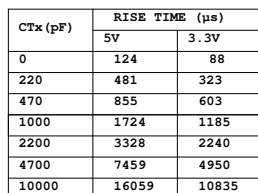


DA10 change P/N from SCA00002900 to SCA00001A00

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The schematic diagram illustrates the internal circuitry of the TPS22966DPUR module. It features three input pins on the left: +1.35V, +1.8V, and +1.8V. The +1.35V input is connected to VIN1 of the U16 (TPS22966DPUR) and VIN1 of the U14 (JUMP_43X118). The +1.8V input is connected to VIN2 of the U16 and VIN2 of the U13 (JUMP_43X118). The module includes several resistors: R435 (1.35V_ON), R436 (1.8VGS_ON), C1014 (0.1u, 0.402 5%, 16V7K), C986 (0.1u, 0.402 5%, 16V7K), C344 (330p, 0.402 50V7K), and C348 (330p, 0.402 50V7K). The output pins on the right are +1.35V_MGM_GFX_OUT1, +1.8VGS_OUT1, and +1.8VGS. The module is labeled with the part number TPS22966DPUR, SON14_2X3, and the manufacturer SA00004MM00.

J13 OPEN DEFAULT

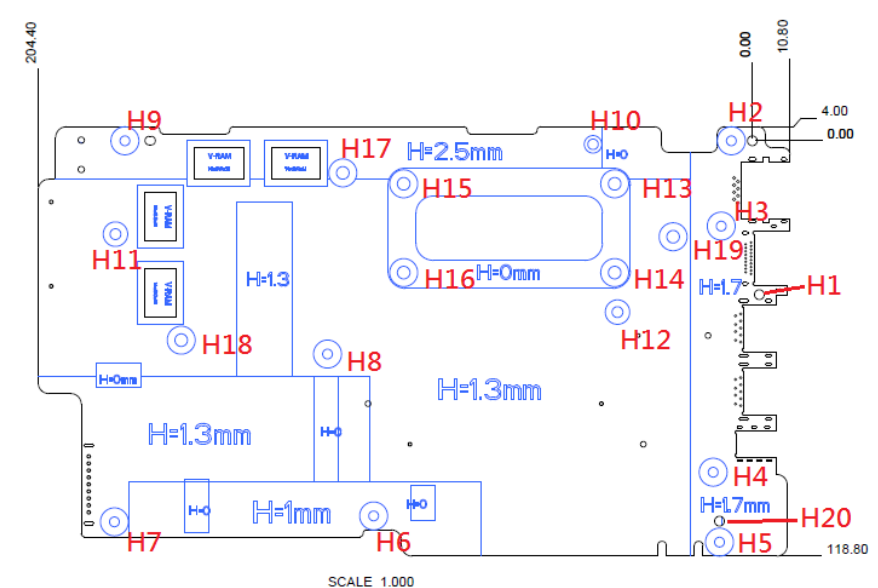
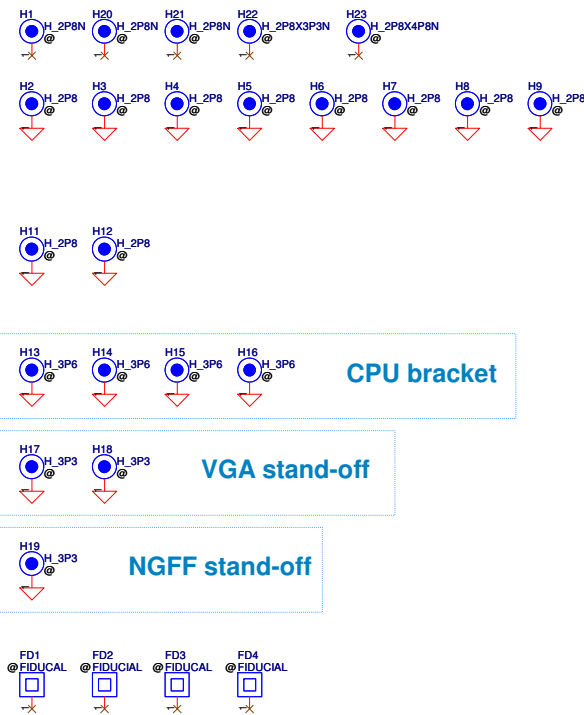
0.95V can be option before VGA core

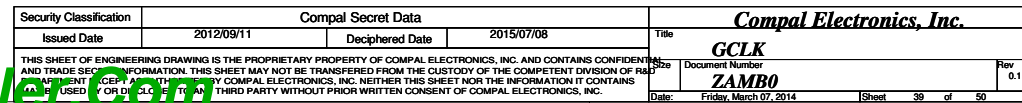
The diagram shows the following signal transitions:

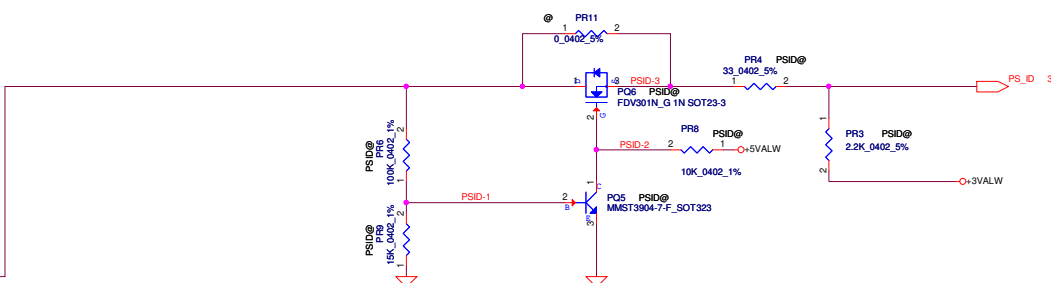
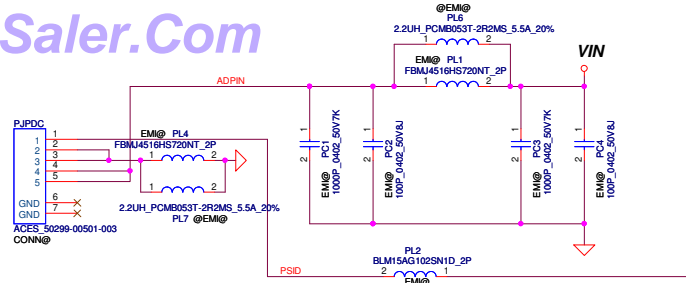
- VGA_ON**: Transitions from low to high.
- +3VSDGPU**: Transitions from low to high.
- VGA_ON_R**: Transitions from high to low.
- +VGA_CORE**: Transitions from low to high.
- VGA_PG**: Transitions from low to high.
- +0.95VSDGPUP**: Transitions from low to high.
- +1.5VSDGPUP**: Transitions from low to high.
- +1.8VSDGPU**: Transitions from low to high.

Red dashed vertical lines indicate the 0.95V threshold for the VGA core, showing that the core voltage is established before the VGA core is enabled.

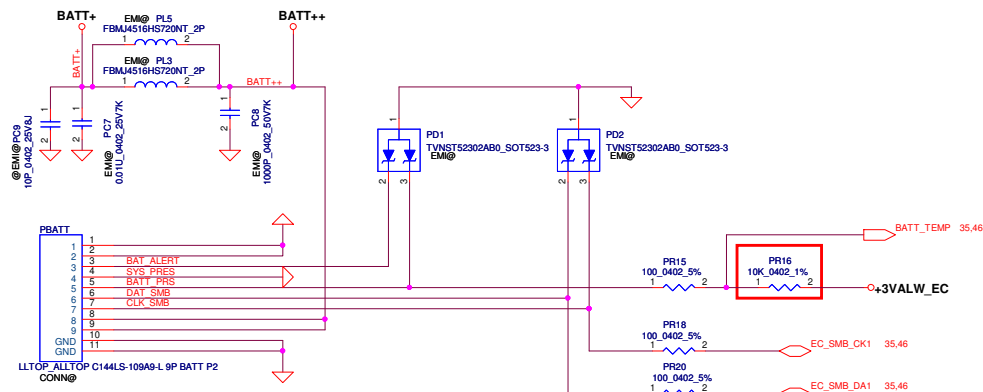
Screw Hole



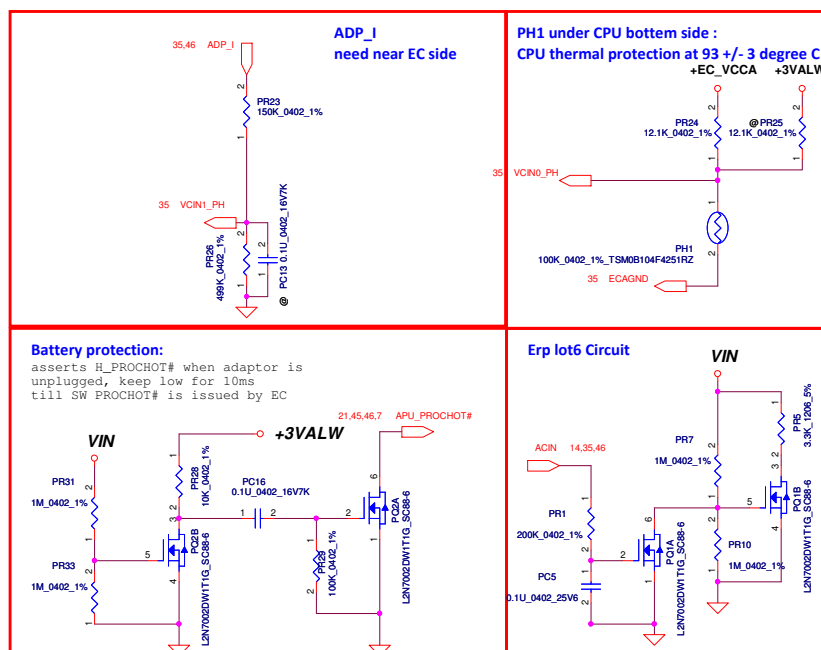




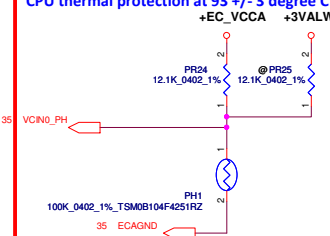
SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1 +
09.BATT2 +



Other component (37.1)

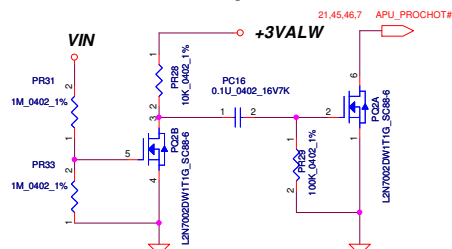


PH1 under CPU bottom side :

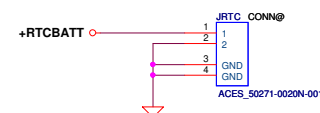
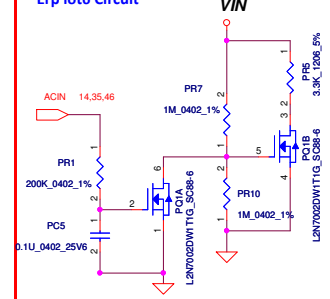


Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



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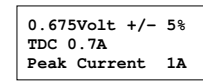
PWR_3.3VALWP/5VALWP

Document Number
74MP0

LAMBO
Friday, March 07

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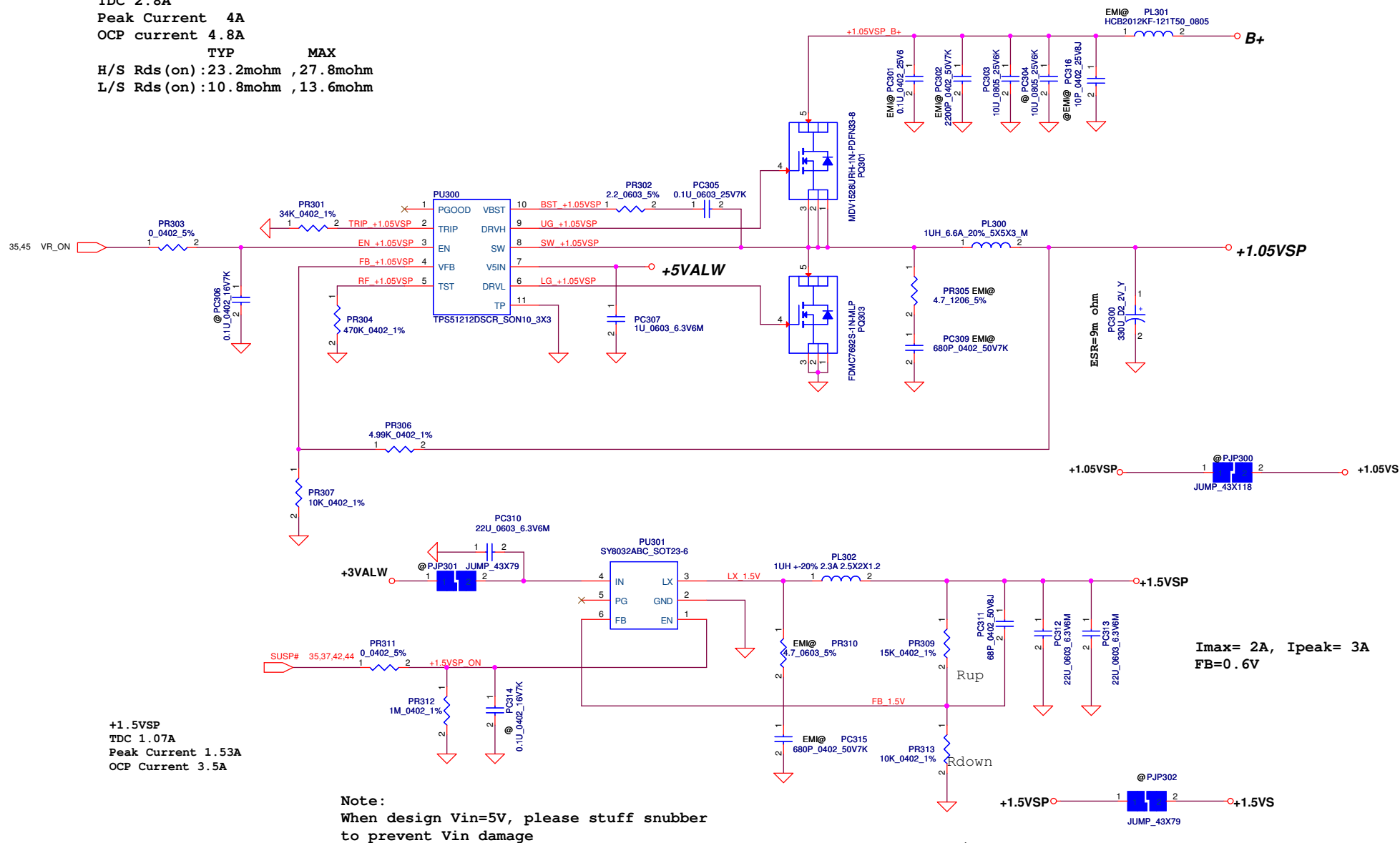
1.35VP
TDC 4A
Peak Current 5.72A
OCP current 6.86A

<p>H/S Rds(on) : 23.2mohm , 27.8mohm L/S Rds(on) : 10.8mohm , 13.6mohm</p>

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1.05VSP
TDC 2.8A
Peak Current 4A
OCP current 4.8A

TYP MAX
H/S Rds(on) : 23.2mohm , 27.8mohm
L/S Rds(on) : 10.8mohm , 13.6mohm



I_{max} = 2A, I_{peak} = 3A
FB = 0.6V

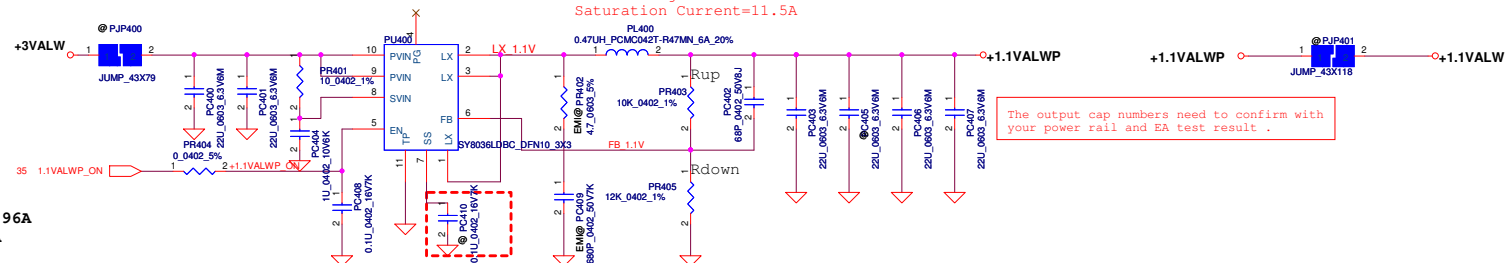
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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FB=0.6V
Note: Iload(max)=6A

4*4 DCR 14~15.5mΩ
Heat Rating Current=6A
Saturation Current=11.5A



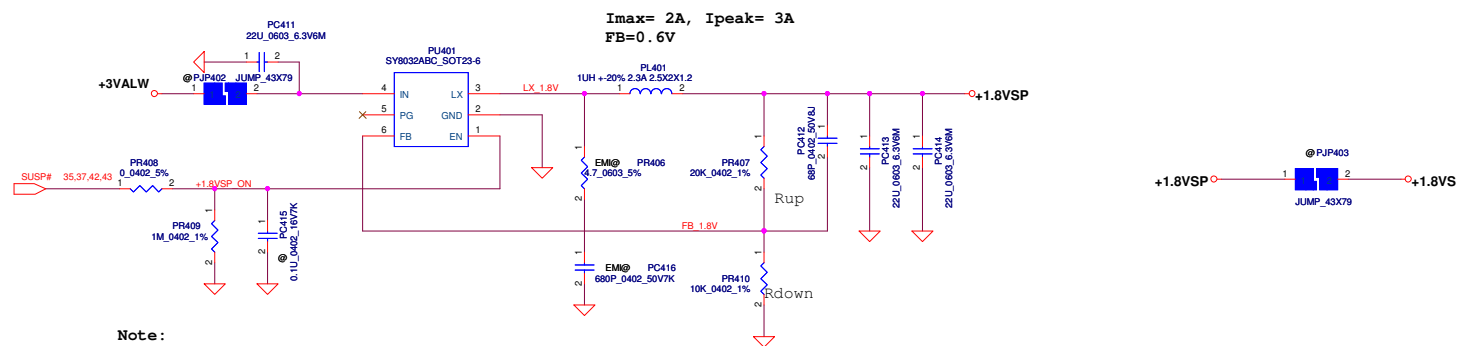
1.1VALWP
TDC 3.47A
Peak Current 4.96A
OCP current 7.5A

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

PC7 to set the Soft Start Time:
CSS=100nF 6ms
Without CSS 0.6ms

$V_{out}=0.6V * (1+R_{up}/R_{down})$

Over voltage IC latch off protection threshold
min=115% type=120% max=125 %
Delay time 10us



+1.8VSP
TDC 1.34A
Peak Current 1.92A
OCP Current 3.5A

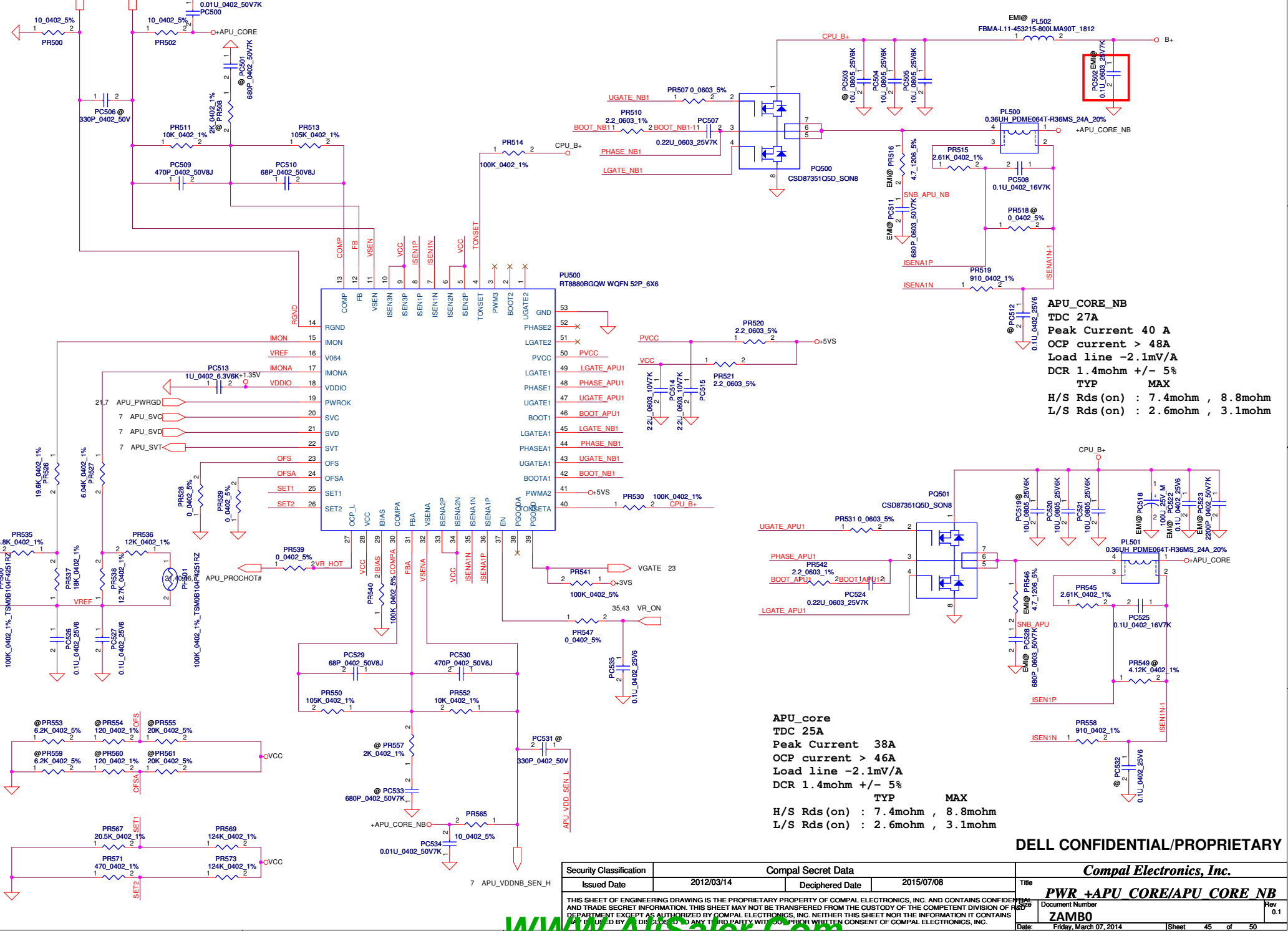
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

I_{max}= 2A, I_{peak}= 3A
FB=0.6V

$V_{out}=0.6V * (1+R_{up}/R_{down})$

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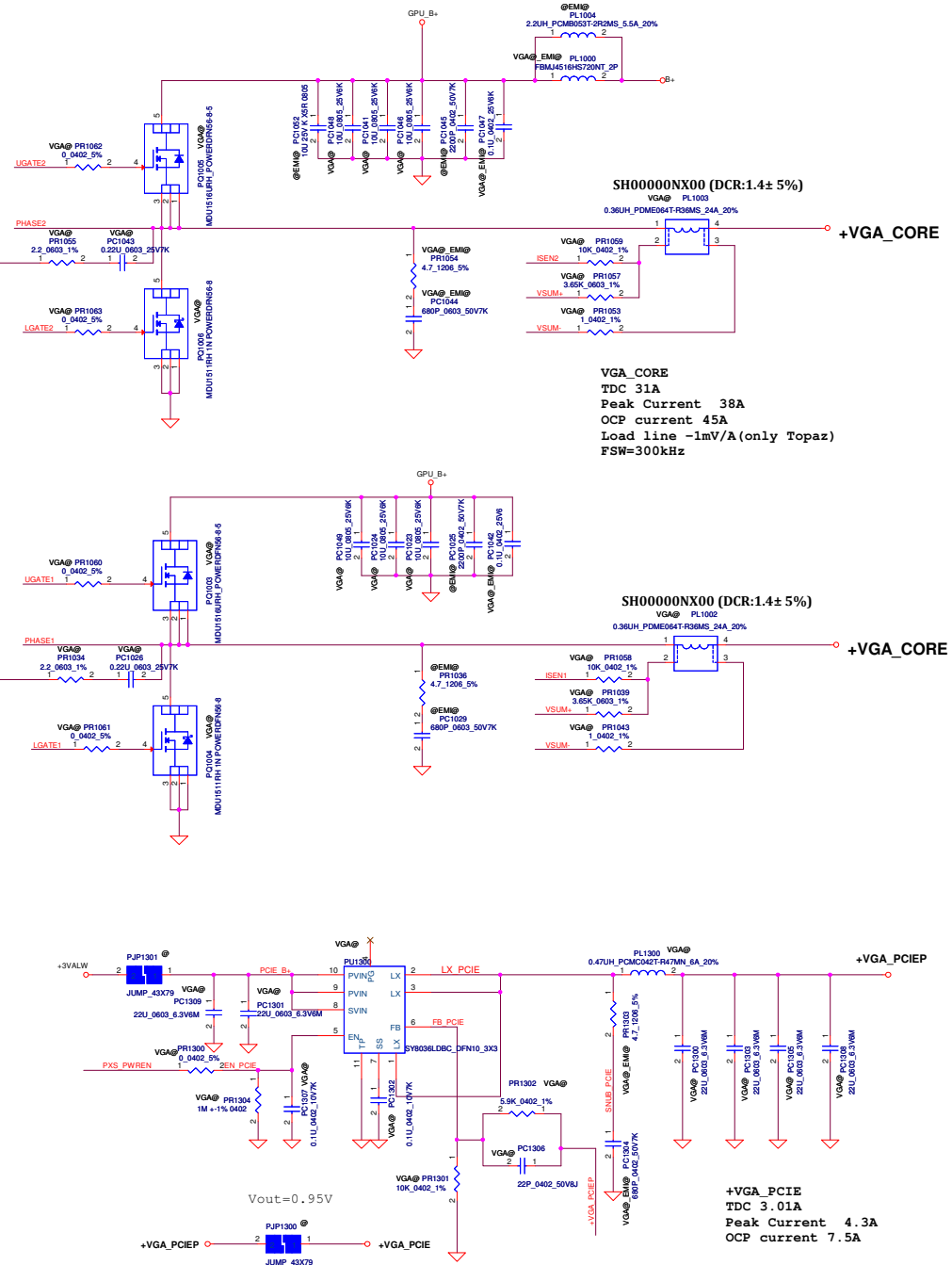
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$$ADP_I = I_{\text{adapter}} * R_{\text{sense}} * \text{Current sense amplifier voltage gain}$$


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PWR-Charger

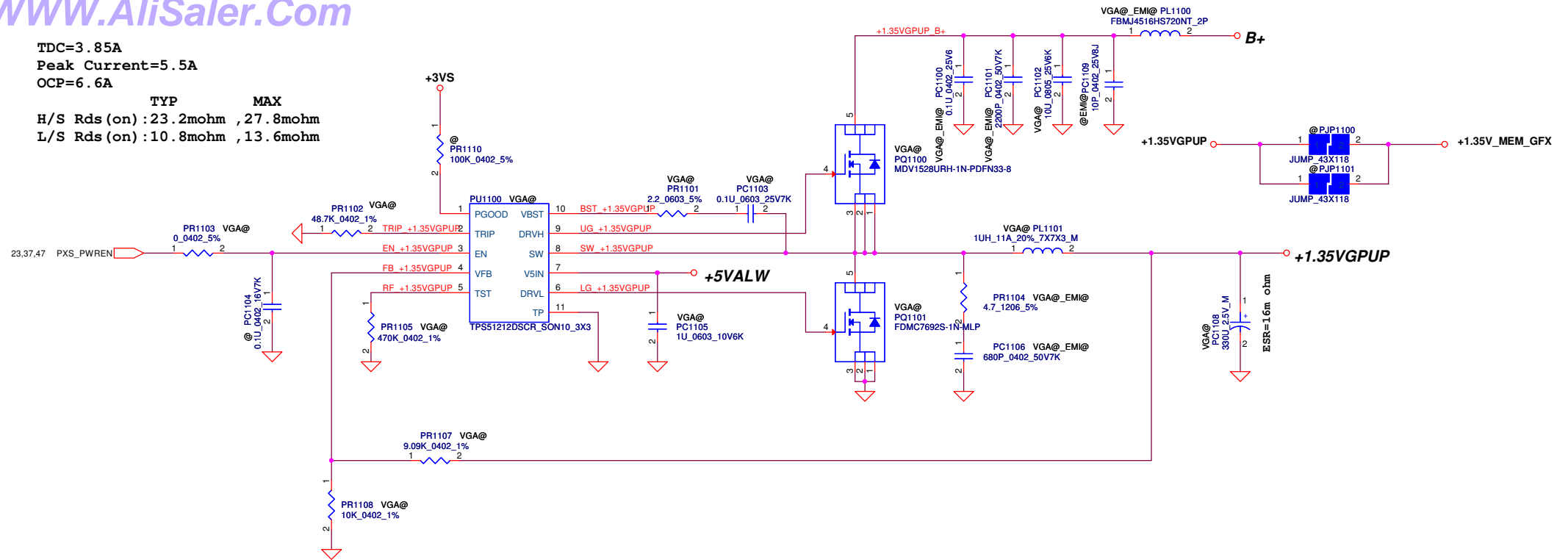
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TDC=3.85A
Peak Current=5.5A
OCP=6.6A

TYP MAX
H/S Rds (on) : 23.2mohm , 27.8mohm
L/S Rds (on) : 10.8mohm , 13.6mohm



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Date: Friday, March 07, 2014				Sheet	50 of 50